3C5000L

V1.2

2024 07

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Haidian District，Beijing

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		3C5000L
		V1.2

1	V1.0	
2	V1.1	
3	V1.2	1-3 HT

: service@loongson.cn

1

1.1

1 32

2 32 64

SoC 3

64 IO

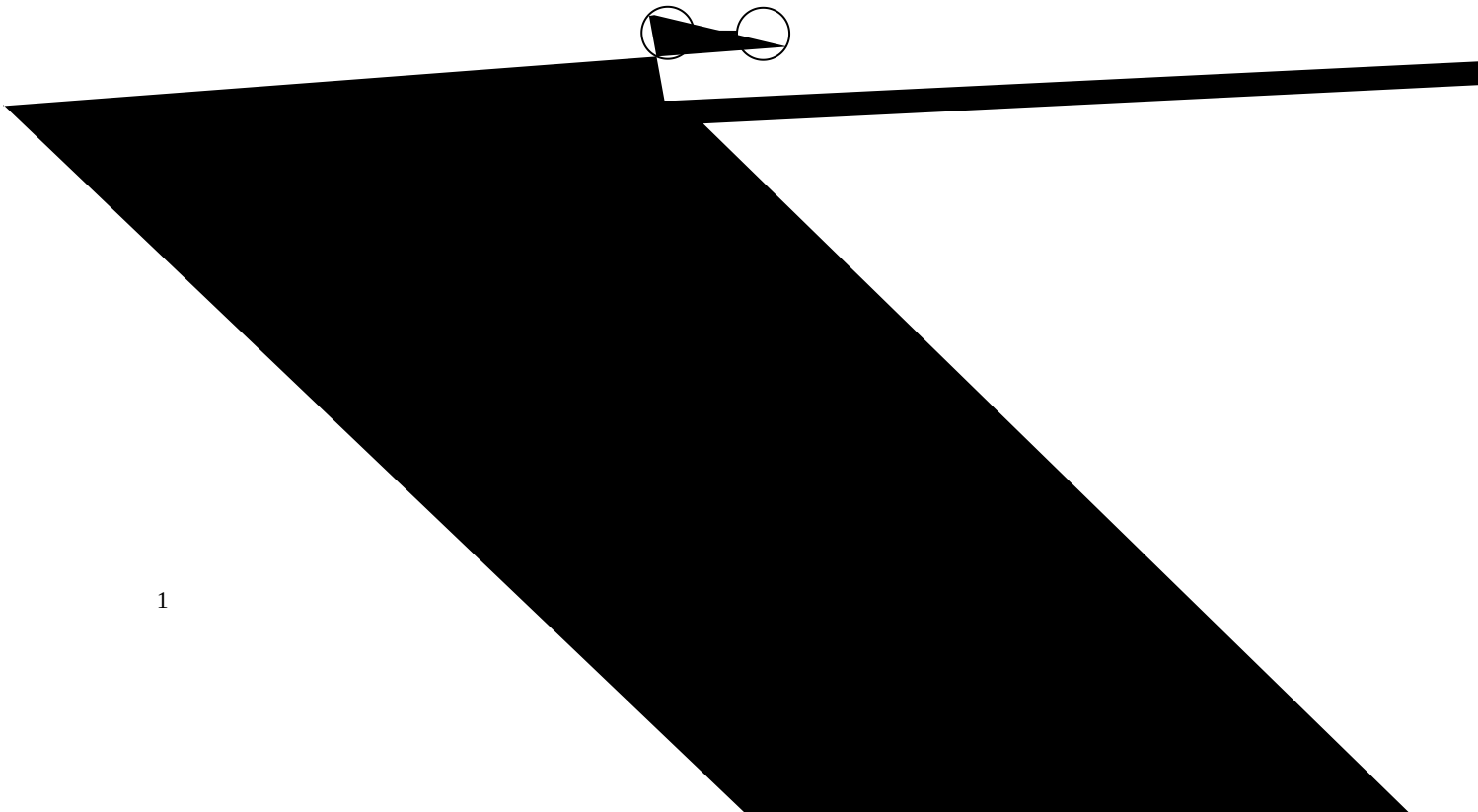
3

2 Cache I/O

3 1- 1 3

8*8

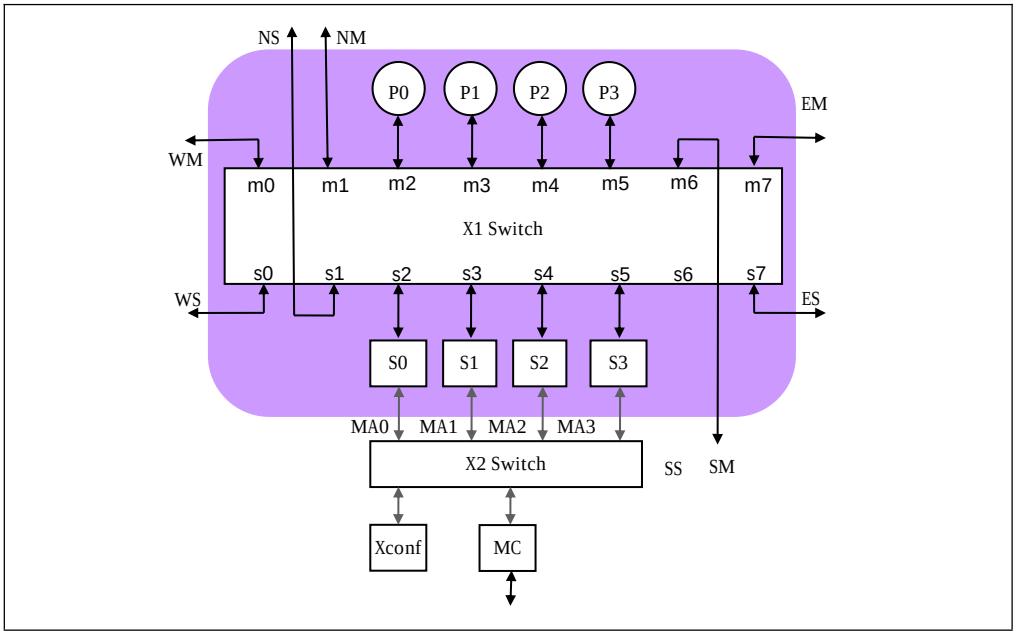
Cache E N W N



3 1-2 AXI

Cache IO AXI X1 Switch X1

Cache X2 Switch X2 Cache



1- 2 3

8*8 X1 Master

P0 P1 P2 P3 Slave interleave Cache

S0 S1 S2 S3 Master/Slave

IO EM/ES SM/SS WM/WS NM/NS

X2 Master Cache Slave

Slave Xconf

X1 X2 IO

1.2 3C5000L

3C5000L 3A5000 BGA-2422

2.0GHz - 2.2GHz

、 16 64 LA464

、 512GFLOPS@2.0GHz

、 64MB Cache

、 I/O DMA Cache

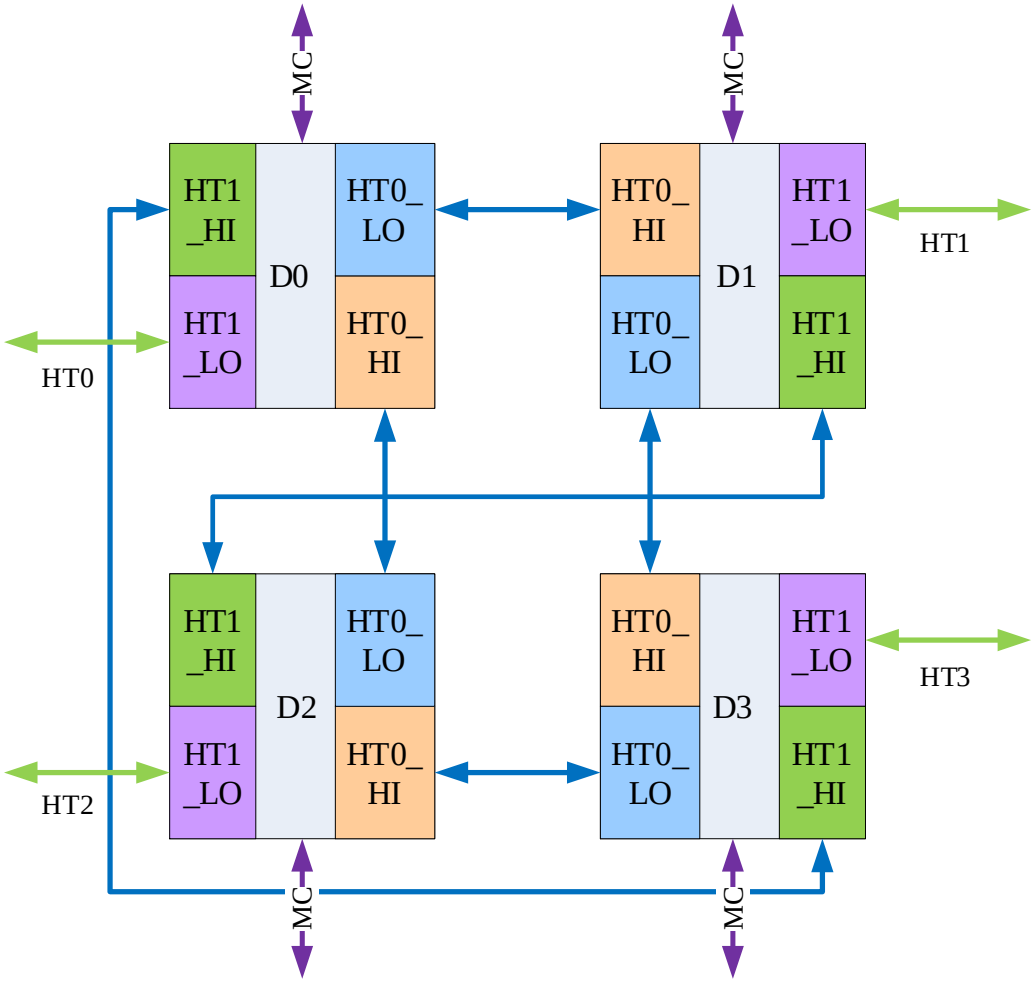
、 4 72 DDR4 DDR4-3200

、 IO 4 HyperTransport HT 3.2GHz

、 3 I2C 1 UART 1 SPI 16 GPIO

3C5000L 2 4

3C5000L 3A5000



1- 3 3C5000L

3A5000

2

<table>
<tr>
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<td>
MEM 1/2
<table>
<tr><th>CLKSEL[3:2]</th><th></th></tr>
<tr><td>2 ‘ b00</td><td>466MHz</td></tr>
<tr><td>2 ‘ b01</td><td>600MHz</td></tr>
<tr><td>2 ‘ b10</td><td>PLL 4.8-6.4GHz</td></tr>
<tr><td>2 ‘ b11</td><td>SYSCLK 100MHz/25MHz</td></tr>
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Main
<table>
<tr><th>CLKSEL[1:0]</th><th></th></tr>
<tr><td>2 ‘ b00</td><td>1GHz</td></tr>
<tr><td>2 ‘ b01</td><td>2GHz</td></tr>
<tr><td>2 ‘ b10</td><td>PLL 4.8-6.4GHz</td></tr>
<tr><td>2 ‘ b11</td><td>SYSCLK 100MHz/25MHz</td></tr>
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<tr>
<td>CHIP_CONFIG[5:0]</td>
<td></td>
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<table>
<tr><td>CHIP_CONFIG[0]</td><td>SE</td></tr>
<tr><td>CHIP_CONFIG[1]</td><td>HT Gen1</td></tr>
<tr><td>CHIP_CONFIG[2]</td><td></td></tr>
<tr><td>CHIP_CONFIG[3]</td><td>HT1-hi</td></tr>
<tr><td>CHIP_CONFIG[4]</td><td>HT1-lo</td></tr>
<tr><td>CHIP_CONFIG[5]</td><td>DCDL</td></tr>
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<tr>
<td>DEV_CONFIG[9:0]</td>
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<tr><td>DEV_CONFIG[0]</td><td></td></tr>
<tr><td>DEV_CONFIG[1]</td><td>D1_HT1_hi</td></tr>
<tr><td>DEV_CONFIG[2]</td><td>D1_HT1_lo</td></tr>
<tr><td>DEV_CONFIG[3]</td><td></td></tr>
<tr><td>DEV_CONFIG[4]</td><td>D2_HT1_hi</td></tr>
<tr><td>DEV_CONFIG[5]</td><td>D2_HT1_hi</td></tr>
<tr><td>DEV_CONFIG[6]</td><td></td></tr>
<tr><td>DEV_CONFIG[7]</td><td>D3_HT1_hi</td></tr>
<tr><td>DEV_CONFIG[8]</td><td>D3_HT1_hi</td></tr>
<tr><td>DEV_CONFIG[9]</td><td></td></tr>
</table>
</td>
</tr>
</table>

3

3

48 4

16 44

3C5000L 4

3.1

4 3C5000L 2/4 CC-NUMA

16 4

3- 1

		[47:44]		
0	0	0	0x0000_0000_0000	0x0FFF_FFFF_FFFF
	1	1	0x1000_0000_0000	0x1FFF_FFFF_FFFF
	2	2	0x2000_0000_0000	0x2FFF_FFFF_FFFF
	3	3	0x3000_0000_0000	0x3FFF_FFFF_FFFF
1	4	4	0x4000_0000_0000	0x4FFF_FFFF_FFFF
	5	5	0x5000_0000_0000	0x5FFF_FFFF_FFFF
	6	6	0x6000_0000_0000	0x6FFF_FFFF_FFFF
	7	7	0x7000_0000_0000	0x7FFF_FFFF_FFFF
2	8	8	0x8000_0000_0000	0x8FFF_FFFF_FFFF
	9	9	0x9000_0000_0000	0x9FFF_FFFF_FFFF
	10	10	0xA000_0000_0000	0xAFFF_FFFF_FFFF
	11	11	0xB000_0000_0000	0xBFFF_FFFF_FFFF
3	12	12	0xC000_0000_0000	0xCFFF_FFFF_FFFF
	13	13	0xD000_0000_0000	0xDFFF_FFFF_FFFF
	14	14	0xE000_0000_0000	0xEFFF_FFFF_FFFF
	15	15	0xF000_0000_0000	0xFFFF_FFFF_FFFF

16 (0x1fe00400) nodemask

0x3

0x7 0xf

3.2

3C5000L 4 16 DDR HT

0x0 0x1000_0000_0000 44

44 cached

4 Cache

3C5000L MC1 HT0 HT1

3- 2

[435 C

4'h3	13:12	4'hb	29:28
4'h4	15:14	4'hc	31:30
4'h5	17:16	4'hd	33:32
4'h6	19:18	4'he	35:34
4'h7	21:20	4'hf	37:36

3C5000L 44

3- 4 44

3.3

3C5000L 4 3A5000

IO-RING Master

Master 8 8

BASE MASK MMAP 64 BASE K MASK

1 MMAP Slave MMAP[4]

MMAP[5] MMAP[6P[5

[7]	[6]	[5]	[4]
	SCACHE/		

: (IN_ADDR & MASK) == BASE

3

SCACHE/ Slave 0 4 0

SCACHE SCID_SEL 4 SCACHE 4

interleave_bit 2 MC

0x1FE0_0000

3- 6

0x2000	CORE0_WIN0_BASE	0x2100	CORE1_WIN0_BASE
0x2008	CORE0_WIN1_BASE	0x2108	CORE1_WIN1_BASE
0x2010	CORE0_WIN2_BASE	0x2110	CORE1_WIN2_BASE
0x2018	CORE0_WIN3_BASE	0x2118	CORE1_WIN3_BASE
0x2020	CORE0_WIN4_BASE	0x2120	CORE1_WIN4_BASE
0x2028	CORE0_WIN5_BASE	0x2128	CORE1_WIN5_BASE
0x2030	CORE0_WIN6_BASE	0x2130	CORE1_WIN6_BASE
0x2038	CORE0_WIN7_BASE	0x2138	CORE1_WIN7_BASE
0x2040	CORE0_WIN0_MASK	0x2140	CORE1_WIN0_MASK
0x2048	CORE0_WIN1_MASK	0x2148	CORE1_WIN1_MASK
0x2050	CORE0_WIN2_MASK	0x2150	CORE1_WIN2_MASK
0x2058	CORE0_WIN3_MASK	0x2158	CORE1_WIN3_MASK
0x2060	CORE0_WIN4_MASK	0x2160	CORE1_WIN4_MASK
0x2068	CORE0_WIN5_MASK	0x2168	CORE1_WIN5_MASK
0x2070	CORE0_WIN6_MASK	0x2170	CORE1_WIN6_MASK
0x2078	CORE0_WIN7_MASK	0x2178	CORE1_WIN7_MASK
0x2080	CORE0_WIN0_MMAP	0x2180	CORE1_WIN0_MMAP
0x2088	CORE0_WIN1_MMAP	0x2188	CORE1_WIN1_MMAP
0x2090	CORE0_WIN2_MMAP	0x2190	CORE1_WIN2_MMAP
0x2098	CORE0_WIN3_MMAP	0x2198	CORE1_WIN3_MMAP
0x20a0	CORE0_WIN4_MMAP	0x21a0	CORE1_WIN4_MMAP
0x20a8	CORE0_WIN5_MMAP	0x21a8	CORE1_WIN5_MMAP
0x20b0	CORE0_WIN6_MMAP	0x21b0	CORE1_WIN6_MMAP
0x20b8	CORE0_WIN7_MMAP	0x21b8	CORE1_WIN7_MMAP
0x2200	CORE2_WIN0_BASE	0x2300	CORE3_WIN0_BASE

0x2208	CORE2_WIN1_BASE	0x2308	CORE3_WIN1_BASE
0x2210	CORE2_WIN2_BASE	0x2310	CORE3_WIN2_BASE
0x2218	CORE2_WIN3_BASE	0x2318	CORE3_WIN3_BASE

0x2478	SCACHE0_WIN7_MASK	0x2578	SCACHE1_WIN7_MASK
0x2480	SCACHE0_WIN0_MMAP	0x2580	SCACHE1_WIN0_MMAP
0x2488	SCACHE0_WIN1_MMAP	0x2588	SCACHE1_WIN1_MMAP
0x2490	SCACHE0_WIN2_MMAP	0x2590	SCACHE1_WIN2_MMAP
0x2498	SCACHE0_WIN3_MMAP	0x2598	SCACHE1_WIN3_MMAP
0x24a0	SCACHE0_WIN4_MMAP	0x25a0	SCACHE1_WIN4_MMAP
0x24a8	SCACHE0_WIN5_MMAP	0x25a8	SCACHE1_WIN5_MMAP
0x24b0	SCACHE0_WIN6_MMAP	0x25b0	SCACHE1_WIN6_MMAP
0x24b8	SCACHE0_WIN7_MMAP	0x25b8	SCACHE1_WIN7_MMAP
0x2600	SCACHE2_WIN0_BASE	0x2700	SCACHE3_WIN0_BASE
0x2608	SCACHE2_WIN1_BASE	0x2708	SCACHE3_WIN1_BASE
0x2610	SCACHE2_WIN2_BASE	0x2710	SCACHE3_WIN2_BASE
0x2618	SCACHE2_WIN3_BASE	0x2718	SCACHE3_WIN3_BASE
0x2620	SCACHE2_WIN4_BASE	0x2720	SCACHE3_WIN4_BASE
0x2628	SCACHE2_WIN5_BASE	0x2728	SCACHE3_WIN5_BASE
0x2630	SCACHE2_WIN6_BASE	0x2730	SCACHE3_WIN6_BASE
0x2638	SCACHE2_WIN7_BASE	0x2738	SCACHE3_WIN7_BASE
0x2640	SCACHE2_WIN0_MASK	0x2740	SCACHE3_WIN0_MASK
0x2648	SCACHE2_WIN1_MASK	0x2748	SCACHE3_WIN1_MASK
0x2650	SCACHE2_WIN2_MASK	0x2750	SCACHE3_WIN2_MASK
0x2658	SCACHE2_WIN3_MASK	0x2758	SCACHE3_WIN3_MASK
0x2660	SCACHE2_WIN4_MASK	0x2760	SCACHE3_WIN4_MASK
0x2668	SCACHE2_WIN5_MASK	0x2768	SCACHE3_WIN5_MASK
0x2670	SCACHE2_WIN6_MASK	0x2770	SCACHE3_WIN6_MASK
0x2678	SCACHE2_WIN7_MASK	0x2778	SCACHE3_WIN7_MASK
0x2680	SCACHE2_WIN0_MMAP	0x2780	SCACHE3_WIN0_MMAP
0x2688	SCACHE2_WIN1_MMAP	0x2788	SCACHE3_WIN1_MMAP
0x2690	SCACHE2_WIN2_MMAP	0x2790	SCACHE3_WIN2_MMAP
0x2698	SCACHE2_WIN3_MMAP	0x2798	SCACHE3_WIN3_MMAP
0x26a0	SCACHE2_WIN4_MMAP	0x27a0	SCACHE3_WIN4_MMAP
0x26a8	SCACHE2_WIN5_MMAP	0x27a8	SCACHE3_WIN5_MMAP
0x26b0	SCACHE2_WIN6_MMAP	0x27b0	SCACHE3_WIN6_MMAP
0x26b8	SCACHE2_WIN7_MMAP	0x27b8	SCACHE3_WIN7_MMAP
-	-	0x2900	IO_L2X_WIN0_BASE
-	-	0x2908	IO_L2X_WIN1_BASE
-	-	0x2910	IO_L2X_WIN2_BASE
-	-	0x2918	IO_L2X_WIN3_BASE

-	-	0x2920	IO_L2X_WIN4_BASE
-	-	0x2928	IO_L2X_WIN5_BASE
-	-	0x2930	IO_L2X_WIN6_BASE
-	-	0x2938	IO_L2X_WIN7_BASE
-	-	0x2940	IO_L2X_WIN0_MASK
-	-	0x2948	IO_L2X_WIN1_MASK
-	-	0x2950	IO_L2X_WIN2_MASK
-	-	0x2958	IO_L2X_WIN3_MASK
-	-	0x2960	IO_L2X_WIN4_MASK
-	-	0x2968	IO_L2X_WIN5_MASK
-	-	0x2970	IO_L2X_WIN6_MASK
-	-	0x2978	IO_L2X_WIN7_MASK
-	-	0x2980	IO_L2X_WIN0_MMAP
-	-	0x2988	IO_L2X_WIN1_MMAP
-	-	0x2990	IO_L2X_WIN2_MMAP
-	-	0x2998	IO_L2X_WIN3_MMAP
-	-	0x29a0	IO_L2X_WIN4_MMAP
-	-	0x29a8	IO_L2X_WIN5_MMAP
-	-	0x29b0	IO_L2X_WIN6_MMAP
-	-	0x29b8	IO_L2X_WIN7_MMAP
0x2a00	HT0_LO_WIN0_BASE	0x2b00	HT0_HI_WIN0_BASE
0x2a08	HT0_LO_WIN1_BASE	0x2b08	HT0_HI_WIN1_BASE
0x2a10	HT0_LO_WIN2_BASE	0x2b10	HT0_HI_WIN2_BASE
0x2a18	HT0_LO_WIN3_BASE	0x2b18	HT0_HI_WIN3_BASE
0x2a20	HT0_LO_WIN4_BASE	0x2b20	HT0_HI_WIN4_BASE
0x2a28	HT0_LO_WIN5_BASE	0x2b28	HT0_HI_WIN5_BASE
0x2a30	HT0_LO_WIN6_BASE	0x2b30	HT0_HI_WIN6_BASE
0x2a38	HT0_LO_WIN7_BASE	0x2b38	HT0_HI_WIN7_BASE
0x2a40	HT0_LO_WIN0_MASK	0x2b40	HT0_HI_WIN0_MASK
0x2a48	HT0_LO_WIN1_MASK	0x2b48	HT0_HI_WIN1_MASK
0x2a50	HT0_LO_WIN2_MASK	0x2b50	HT0_HI_WIN2_MASK
0x2a58	HT0_LO_WIN3_MASK	0x2b58	HT0_HI_WIN3_MASK
0x2a60	HT0_LO_WIN4_MASK	0x2b60	HT0_HI_WIN4_MASK
0x2a68	HT0_LO_WIN5_MASK	0x2b68	HT0_HI_WIN5_MASK
0x2a70	HT0_LO_WIN6_MASK	0x2b70	HT0_HI_WIN6_MASK
0x2a78	HT0_LO_WIN7_MASK	0x2b78	HT0_HI_WIN7_MASK
0x2a80	HT0_LO_WIN0_MMAP	0x2b80	HT0_HI_WIN0_MMAP
0x2a88	HT0_LO_WIN1_MMAP	0x2b88	HT0_HI_WIN1_MMAP

0x2e38	HT1_LO_WIN7_BASE	0x2f38	HT1_HI_WIN7_BASE
0x2e40	HT1_LO_WIN0_MASK	0x2f40	HT1_HI_WIN0_MASK
0x2e48	HT1_LO_WIN1_MASK	0x2f48	HT1_HI_WIN1_MASK
0x2e50	HT1_LO_WIN2_MASK	0x2f50	HT1_HI_WIN2_MASK
0x2e58	HT1_LO_WIN3_MASK	0x2f58	HT1_HI_WIN3_MASK
0x2e60	HT1_LO_WIN4_MASK	0x2f60	HT1_HI_WIN4_MASK
0x2e68	HT1_LO_WIN5_MASK	0x2f68	HT1_HI_WIN5_MASK
0x2e70	HT1_LO_WIN6_MASK	0x2f70	HT1_HI_WIN6_MASK
0x2e78	HT1_LO_WIN7_MASK	0x2f78	HT1_HI_WIN7_MASK
0x2e80	HT1_LO_WIN0_MMAP	0x2f80	HT1_HI_WIN0_MMAP
0x2e88	HT1_LO_WIN1_MMAP	0x2f88	HT1_HI_WIN1_MMAP
0x2e90	HT1_LO_WIN2_MMAP	0x2f90	HT1_HI_WIN2_MMAP
0x2e98	HT1_LO_WIN3_MMAP	0x2f98	HT1_HI_WIN3_MMAP
0x2ea0	HT1_LO_WIN4_MMAP	0x2fa0	HT1_HI_WIN4_MMAP
0x2ea8	HT1_LO_WIN5_MMAP	0x2fa8	HT1_HI_WIN5_MMAP
0x2eb0	HT1_LO_WIN6_MMAP	0x2fb0	HT1_HI_WIN6_MMAP
0x2eb8	HT1_LO_WIN7_MMAP	0x2fb8	HT1_HI_WIN7_MMAP

xbar 2 IO-RING 4 Scache 4

0x24xx 5 6 7 IO-RING 9

4 5 6 7 9

BASE MASK MMAP 64 BASE K MASK

1 MMAP

3- 7MMAP

[63:48]	[47 10]	[7 4]	[3 0]

3- 8

0-3	Scache0-3
4-5	MC0-1
a	HT0_lo
b	HT0_hi
c	SE
d	MISC

e	HT1_lo
f	HT1_hi

3- 9 MMAP

[7]	[6]	[5]	[4]
	DDR 0 “ interleave_bit CSR0x0400 ” 10		

!

4

3C5000L

3C5000L 4

0x1fe00000

IOCSR

CSR[A][B] A IOCSR B B

4.1 0x0000

0x1fe00000 0x0000

4- 1

7:0	Version	R	8'h11	

4.2 0x0008

0x0008

4- 2

0	Centigrade	R	1'b1	1 CSR[0x428]
1	Node counter	R	1'b1	1 CSR[0x408]
2	MSI	R	1'b1	1 MSI
3	EXT_IOI	R	1'b1	1 EXT_IOI
4	IPI_percore	R	1'b1	1 CSR IPI
5	Freq_percore	R	1'b1	1 CSR
6	Freq_scale	R	1'b1	1
7	DVFS_v1	R	1'b1	1 v1
8	Tsensor	R	1'b1	1

9		R	1’b1	
10		R	1’b0	
11	Guest Mode	WR	1’b0	KVM

4.3 0x0010

0x0010

4- 3

63:0	Vendor	R	0x6e6f7367_6e6f6f4c	“ Loongson ”

4.4 0x0020

0x0020

4- 4

63:0	ID	R	0x00003030_30354133	“ 3A5000 ”

4.5 0x0180

0x0180

4- 5

0		RW	1’b0	
1		RW	1’b0	
3:2		RW	2’b0	
4	MC0_disable_confspace	RW	1’b0	MC0 DDR
5	MC0_defult_confspace	RW	1’b1	
6	MCA0 clock en	RW	1’b1	MCA0
7	MC0_resetn	RW	1’b1	MC0
8	MC0_clken	RW	1’b1	MC0
9	MC1_disable_confspace	RW	1’b0	MC1 DDR
10	MC1_defult_confspace	RW	1’b1	
11	MCA1 clock en	RW	1’b1	MCA1
12	MC1_resetn	RW	1’b1	MC1

13	MC1_clken	RW	1’b1	MC1
26:24	HT0_freq_scale_ctrl	RW	3’b011	HT 0
27	HT0_clken	RW	1’b1	HT0
30:28	HT1_freq_scale_ctrl	RW	3’b011	HT 1
31	HT1_clken	RW	1’b1	HT1
42:40	Node_freq_ ctrl	RW	3’b111	
43	-	RW	1’b1	
63:56	Cpu_version	R	2’h3D	CPU

4.6 0x0188

0x0188

4- 6

15:0				
19:16	HT sideband	RW	2’b0	HT
23:20	I2C	RW	2’b0	I2C
27:24	UART	RW	2’b0	UART
31:28	SPI	RW	2’b0	SPI
35:32	GPIO	RW	2’b0	GPIO
39:36	SE UART	RW	2’b0	SE UART
43:40	SE SPI	RW	2’b0	SE SPI
47:44	SE I2C	RW	2’b0	SE I2C
51:48	SE SCI	RW	2’b0	SE SCI
55:52	SE RNG	RW	2’b0	SE RNG
59:56	SE GPIO	RW	2’b0	SE GPIO

4.7 0x0190

0x0190

4- 7

31:0		R		
37:32	Chip_config	R		
47:38	Sys_clkseli	R		
55:48	Bad_ip_core	R		core7-core0

57:56	Bad_ip_ddr	R		2 DDR
61:60	Bad_ip_ht	R		2 HT

4.8 0x0198

0x0198

4- 8

15:0		R		
19:16		R		
20	dotest	R		Dotest
21	iccc_en	R		Iccc_en
23:22		R		
24	Thsens0_overflow	R		0
25	Thsens1_overflow	R		1
31:26				
47:32	Thsens0_out	R		0 =Thens0_out *731/0x4000 - 273 -40 – 125
63:48	Thsens1_out	R		1 =Thens1_out *731/0x4000 - 273 -40 – 125

4.9 0x01B0

CLKSEL 2.2

CLKSEL

Mem Clock 4 mem div Mem Clock

4 2 mem div Mem Clock

2 mem div Mem Clock

2 4

Node Clock

DIV_REFC DIV_LOOPC DIV_OUT

/DIV_REFC * DIV_LOOPC / DIV_OUT

100MHz 25MHz

1) SEL_PLL_* SOFT_SET_PLL

0

2) SOFT_SET_PLL 1

3) LOCKED_* 1

4) SEL_PLL_* 1

Main Clock Main Clock node clock core clock

0x1b0

4- 9

0	SEL_PLL_NODE	RW	0x0	1 Node PLL 0 Node SYS CLOCK
1		RW	0x0	
2	SOFT_SET_PLL	RW	0x0	PLL
3	BYPASS_L1	RW	0x0	Bypass L1 PLL
7:4	-	RW	0x0	
8	VDDA_LDO_EN	RW	0x0	VDDA LDO
9	VDDD_LDO_EN	RW	0x0	VDDD LDO
11:10	-			
12	DACPD_L2	RW	0x0	L2 DACPD
13	DSMPD_L2	RW	0x0	L2 DSMPD
15:14		RW	0x0	
16	LOCKED_L1	R	0x0	L1 PLL
18:17	-	R	0x0	
19	PD_L1	RW	0x0	L1 PLL
21:20		RW	0x0	
22	L2_SEL	RW	0x0	L2
25:23		RW	0x0	
31:26	L1_DIV_REFC	RW	0x1	L1 PLL
40:32	L1_DIV_LOOPC	RW	0x1	L1 PLL
41				
47:42	L1_DIV_OUT	RW	0x1	L1 PLL
53:48	L2_DIV_REFC	RW		
63:54	L2_DIV_LOOPC	RW		

69:64	L2_DIV_OUT	RW		
95:70	-	RW		
119:96	L2_FRAC	RW		
122:120	VDDA_LDO_CTRL	RW		
123	VDDA_LDO_BYPASS	RW		
126:124	VDDD_LDO_CTRL	RW		
127:124	VDDD_LDO_BYPASS	RW		
	-	RW		

PLL ouput = clk_ref /div_refc * div_loopc / div_out

PLL clk_ref/div_refc 25/50/100MHz 50MHz VCO

4.8GHz – 6.4GHz PLL

div_loopc 255 div_out 1/2/4/6

6 3/5

Mem Clock Mem Clock DDR

1/2 0x1c0

4- 10

[0]	SEL _MEM_PLL	RW	0x0	1 MEM PLL 0 MEM SYS CLOCK
[1]	SOFT_SET_MEM_PLL	RW	0x0	MEM PLL
[2]	BYPASS_MEM_PLL	RW	0x0	Bypass MEM_PLL
[3]	MEMDIV_RESETn	RW	0x1	
[5:4]	MEMDIV_MODE	RW		00 01 2 10 4 11
[6]	LOCKED_MEM_PLL	R	0x0	MEM_PLL
[7]	PD_MEM_PLL	RW	0x0	MEM PLL
[13:8]	MEM_PLL_DIV_REFC	RW	0x1	MEM PLL NODE NODE_CLOCK_SEL 1
[23:14]	MEM_PLL_DIV_LOOPC	RW	0x41	MEM PLL
[29:24]	MEM_PLL_DIV_OUT	RW	0x0	MEM PLL
[30]	NODE_CLOCK_SEL	RW	0x0	0 MEM_PLL MEM 1 NODE_CLOCK
[31]	-			

[34:32]	VDDA_LDO_CTRL	RW		
[35]	VDDA_LDO_BYPASS	RW		
[38:36]	VDDD_LDO_CTRL	RW		
[39]	VDDD_LDO_BYPASS	RW		
[40]	VDDA_LDO_EN	RW		
[41]	VDDD_LDO_EN	RW		
		RW		

4.10 0x01D0

100ns 0x01d0

4- 11

2:0	core0_freqctrl	RW	0x7	0
3	core0_en	RW	0x1	0
6:4	core1_freqctrl	RW	0x7	1
7	core1_en	RW	0x1	1
10:8	core2_freqctrl	RW	0x7	2
11	core2_en	RW	0x1	2
14:12	core3_freqctrl	RW	0x7	3
15	core3_en	RW	0x1	3
			:	+1 /8

4.11 0x01D8

resetn 0

resetn_pre 0 500 resetn_pre 1 resetn 1

0x01d8

4- 12

0	Core0_resetn_pre	RW	0x1	0
1	Core0_resetn	RW	0x1	0
2	Core1_resetn_pre	RW	0x1	1

3	Core1_resetn	RW	0x1	1
4	Core2_resetn_pre	RW	0x1	2
5	Core2_resetn	RW	0x1	2
6	Core3_resetn_pre	RW	0x1	3
7	Core3_resetn	RW	0x1	3

4.12 0x0400

0x0400

4- 13

3:0	scid_sel	RW	0x0	
7:4	Node_mask	RW	0xF	
8	xrouter_en	RW	0x0	HT1
9	disable_0x3ff0	RW	0x0	0x3ff0_0000
10	Fast_path_36_en	RW	0x0	36 8
11	Fast_path_27_en	RW	0x0	27 8
12	mcc_en	RW	0x0	MCC
14	Scahe_1MB	RW		Scache
19:16	ccsd_id	RW	0x0	
24	ccsd_en	RW	0x0	
31:30	mc_en	RW	0x3	MC
37:32	interleave_bit	RW	0x0	
39	interleave_en	RW	0x0	
43:40	ht_control	R		Ht
47:44	ht_reg_disable	RW	0x0	ht HT HT
60:56	Line_ag_cfg	RW	0x0	

4.13 0x0420

0x0420

4- 14

46:44	freqscale_stable	RW	0x0	Stable clock
47	clken_stable	RW	0x0	Stable clock
48	EXT_INT_en	RW	0x0	IO
49	INT_encode	RW	0x0	
53:52				
54				
57:56	thsensor_sel	RW	0x0	
62:60	Auto_scale	R	0x0	
63	Auto_scale_doing	R	0x0	

4.14 0x0428

0x0428

CSR[0x0008][0]

4- 15

7:0	Centigrade temperature	RO	0x0	
63:8		RW	0x0	

4.15 SRAM 0x0430

Sram 0x0430

4- 16 SRAM

31:0	sram_ctrl	RW	0x0	Sram
63:32		RW	0x0	

4.16 FUSE0 0x0460

Fuse0 0x0460

4- 17 FUSE

127:0	Fuse_0	RW	0x0	

4.17 FUSE1 0x0470

Fuse1 0x0470

4- 18 FUSE

127:0	Fuse_1	RW	0x0	

5

3C5000L 4 SYS_CLOCK[N]
SYS_CLOCK_N
3C5000L HT LA132
3C5000L 1/n
3C5000L 4
0x1fe00000 IOCSR

5.1

SYS_CLOCK[N] 100MHz 25MHz
CLKSEL[4]
HT PHY SYS CLOCK PHY 200MHz
CLKSEL[8] SYS CLOCK 25MHz HT PHY 3.2GHz
3C5000L

5- 1

Boot Clock	SYS_CLOCK	*1			SPI UART I2C
Main Clock	SYS PLL	PLL			SYS PLL Node Clock Core Clock HTcore Clock LA132 Clock Mem Clock Stable Clock
Node Clock	Main Clock	*1			HT
Core0 Clock	Main Clock	*1			Core0
Core1 Clock	Main Clock	*1			Core1
Core2 Clock	Main Clock	*1			Core2
Core3 Clock	Main Clock	*1			Core3
HTcore0 Clock	Node Clock	*1			HT0 1GHz
HTcore1 Clock	Node Clock	*1			HT1 1GHz

LA132 Clock	Main Clock	*1			LA132 1GHz
Stable Clock	SYS_CLOCK	*1			
Mem Clock	MEM PLL	PLL			
	Main Clock	/2 /4 /8			

5.2

5.2.1

3C5000L 4

3A3000

100ns

0x1fe00000 0x01d0

5- 2

2:0	core0_freqctrl	RW	0x7	0
3	core0_en	RW	0x1	0
6:4	core1_freqctrl	RW	0x7	1
7	core1_en	RW	0x1	1
10:8	core2_freqctrl	RW	0x7	2
11	core2_en	RW	0x1	2
14:12	core3_freqctrl	RW	0x7	3
15	core3_en	RW	0x1	3
			:	+1 /8

3A3000 3C5000L

“ +1 /8 ” “ 1/ +1 ”

“ ” 0x1fe00000 0x0420

5- 3

35:32	freqscale_mode_core	RW	0x0	

				0: (n+1)/8 1: 1/(n+1)

5.2.2

3C5000L

“ ”

0x1fe00000 0x0420

5- 4

22	freqscale_percore	RW	0x0	
23	clken_percore	RW	0x0	

freqscale_percore 1 freqscale

freqscale_mode clken_percore 1

clken

0x1050

5- 5

4	freqscale_mode	RW	0x0	0: (n+1)/8 1: 1/(n+1)
3	clken	RW	0x0	
2:0	freqscale	RW	0x0	

5.3

clken

5.3.1

0x1fe00000 0x0180

5- 6

42:40	Node0_freq_ ctrl	RW	3’b111	0

“ +1 /8 ” “ 1/ +1 ” “

” 0x1fe00000 0x0420

5- 7

36	freqscale_mode_node	RW	0x0	0: (n+1)/8 1: 1/(n+1)

5.3.2

4

GATE

EN 1

SEL 3C5000L

FREQ freqscale_mode_node

0 (FREQ+1)/8 1

26:24	HT0_freq_scale	RW	3’b111	HT 0
27	HT0_clken	RW	1’b1	HT0
30:28	HT1_freq	RW	3’b111	HT 1
31	HT1_clken	RW	1’b1	HT1

HT

“ +1 /8 ” “ 1/ +1 ” “

” 0x1fe00000 0x0420

HT core clock Node clock Node clock

5- 10

39:38	freqscale_mode_HT	RW	0x0	HT 0: (n+1)/8 1: 1/(n+1)

5.5 Stable Counter

Stable Counter

0x1fe00000 0x0420

5- 11

20	stable_sel	RW	0x0	0 SYS CLOCK 1 NODE CLOCK
21	stable_reset	RW	0x0	1 0 Stable clock
40	freqscale_mode_stable	RW	0x0	0: (n+1)/8 1: 1/(n+1)
46:44	freqscale_stable	RW	0x0	Stable clock
47	clken_stable	RW	0x0	

5- 12 GPIO

31:0	GPIO_OEn	RW	32’hffffffff	GPIO
63:32	GPIO_FUNC_En	RW	32’hffff0000	GPIO

6

3C5000L

counter/compare stable counter node counter

stable counter node counter

6.1 Stable Counter

3C5000L stable counter Stable counter

3C5000L

stable counter

Stable couter

6.1.1 Stable Timer

Stable counter counter

timer Stable counter Stable timer

rdhwr DRDTIME

load/store CSR

6- 1

Core0_timer_config	0x1060	RW	0
Core0_timer_ticks	0x1070	R	0
Core1_timer_config	0x1160	RW	1
Core1_timer_ticks	0x1170	R	1
Core2_timer_config	0x1260	RW	2
Core2_timer_ticks	0x1270	R	2
Core3_timer_config	0x1360	RW	3
Core3_timer_ticks	0x1370	R	3

6- 2

percore_timer_config	0x1060	RW	
percore_timer_ticks	0x1070	R	

6- 3

timer_config				
63	1	RW	0x1	1 1
62	Periodic	RW	0x0	1 0 timer_config InitVal
61	Enable	RW	0x0	1
47:0	InitVal	RW	0x0	
timer_ticks				
63:48	0	R	0x0	0
47:0	Ticks	R	0x0	48'hffff_ffff_ffff

6.1.2 Stable Counter

Stable counter

Stable counter

0x1fe00000 0x0420

6- 4

20	stable_sel	RW	0x0	0 SYS CLOCK 1 NODE CLOCK
21	stable_reset	RW	0x0	1 0
40	freqscale_mode_stable	RW	0x0	Stable clock 0: (n+1)/8 1: 1/(n+1)
46:44	freqscale_stable	RW	0x0	Stable clock
47	clken_stable	RW	0x0	Stable clock

BIOS Stable counter MCSR

CPUCFG.0x4 CPUCFG.0x5 8.1 CPUCFG.0x4

Hz CPUCFG.0x5[31:16] CPUCFG.0x5[15:0]

BIOS CCFreq*CFM/CFD

Stable Counter

6.1.3 Stable Counter

Counter 2

counter 100ns

SYS_CLK

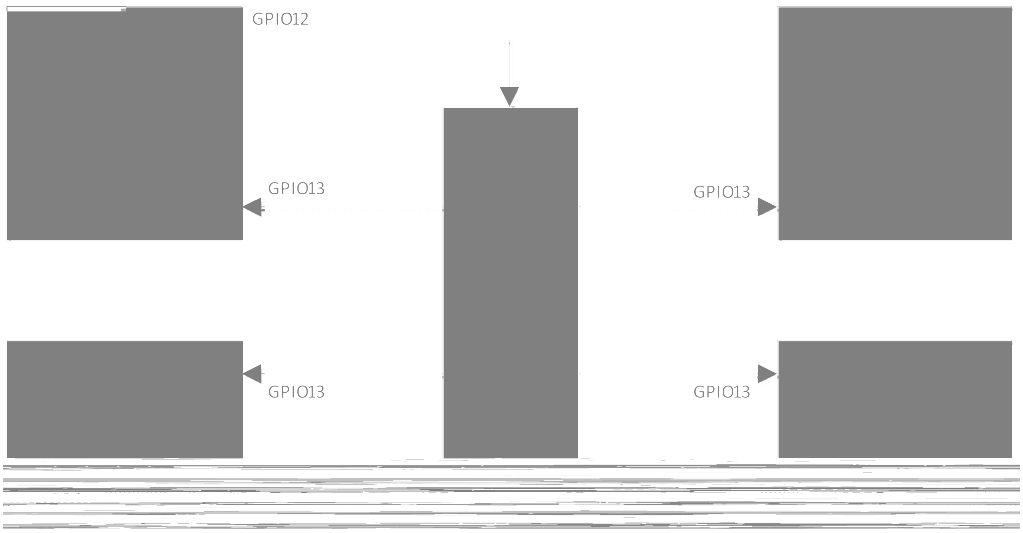
Stable counter

GPIO 0 GPIO12 0

GPIO13 Stable counter

Stable counter Stable counter GPIO12

BIOS



3C5000L

7 GPIO

3C5000L 32 GPIO

GPIO

0x1fe00000

7.1 0x0500

0x1fe00000 0x0500

7- 1

31:0	GPIO_OEn	RW	32'hffffffff	GPIO
63:32	GPIO_FUNC_En	RW	32'hffff0000	GPIO

7.2 0x0508

0x1fe00000 0x0508

7- 2

31:0	GPIO_O	RW	32'h0	GPIO
63:32	GPIO_I	RO	32'h0	GPIO

7.3 0x0510

0x1fe00000 0x0510

7- 3

31:0	GPIO_INT_Pol	RW	32'h0	GPIO 0 - 1 -
63:32	GPIO_INT_en	RW	32'h0	GPIO

7.4 GPIO

3C5000L GPIO

GPIO00 – GPIO15 GPIO

IO

GPIO16 – GPIO31 HT HT

IO HT0/1_Hi/Lo_Hostmode

HT IO GPIO

GPIO

7- 4 GPIO

GPIO			
0	GPIO00	SPI_CSn1	GPIO
1	GPIO01	SPI_CSn2	GPIO
2	GPIO02	UART1_RXD	GPIO
3	GPIO03	UART1_TXD	GPIO
4	GPIO04	UART1_RTS	GPIO
5	GPIO05	UART1_CTS	GPIO
6	GPIO06	UART1_DTR	GPIO
7	GPIO07	UART1_DSR	GPIO
8	GPIO08	UART1_DCD	GPIO
9	GPIO09	UART1_RI	GPIO
10	GPIO10	-	GPIO
11	GPIO11	-	GPIO
12	GPIO12	-	GPIO
13	GPIO13	SCNT_RSTn	GPIO
14	GPIO14	PROCHOTn	GPIO
15	GPIO15	THERMTRIPn	GPIO
16	HT0_LO_POWEROK	GPIO16	HT0_LO_POWEROK
17	HT0_LO_RSTn	GPIO17	HT0_LO_RSTn
18	HT0_LO_LDT_REQn	GPIO18	HT0_LO_LDT_REQn
19	HT0_LO_LDT_STOPn	GPIO19	HT0_LO_LDT_STOPn

20	HT0_HI_POWEROK	GPIO20	HT0_HI_POWEROK
21	HT0_HI_RSTn	GPIO21	HT0_HI_RSTn
22	HT0_HI_LDT_REQn	GPIO22	HT0_HI_LDT_REQn
23	HT0_HI_LDT_STOPn	GPIO23	HT0_HI_LDT_STOPn
24	HT1_LO_POWEROK	GPIO24	HT1_LO_POWEROK
25	HT1_LO_RSTn	GPIO25	HT1_LO_RSTn
26	HT1_LO_LDT_REQn	GPIO26	HT1_LO_LDT_REQn
27	HT1_LO_LDT_STOPn	GPIO27	HT1_LO_LDT_STOPn
28	HT1_HI_POWEROK	GPIO28	HT1_HI_POWEROK
29	HT1_HI_RSTn	GPIO29	HT1_HI_RSTn
30	HT1_HI_LDT_REQn	GPIO30	HT1_HI_LDT_REQn
31	HT1_HI_LDT_STOPn	GPIO31	HT1_HI_LDT_STOPn

7.5 GPIO

3C5000L GPIO

GPIO00	GPIO08	GPIO16	GPIO24	0
GPIO01	GPIO09	GPIO17	GPIO25	1
GPIO02	GPIO10	GPIO18	GPIO26	2
GPIO03	GPIO11	GPIO19	GPIO27	3
GPIO04	GPIO12	GPIO20	GPIO28	4
GPIO05	GPIO13	GPIO21	GPIO29	5
GPIO06	GPIO14	GPIO22	GPIO30	6
GPIO07	GPIO15	GPIO23	GPIO31	7

GPIO GPIO_INT_en GPIO_INT_POL

0x1fe00000 0x0510

7- 5

31:0	GPIO_INT_Pol	RW	32'h0	GPIO 0 -

				1 -
63:32	GPIO_INT_en	RW	32’h0	GPIO

GPIO

POL 0 1

8 LA464

LA464 64

3C5000L

LA464 Cache AXI Cache

LA464

- LoongArch
-
- 256 8 4
- 256 64 48
-
- 64 8 2048 2112 TLB 64 TLB

- Cache Cache 64KB 4
- Victim Cache Cache 256KB 16
- Non-blocking Load-Speculation
- Cache
- Cache Cache ECC
- JTAG

8.1 3C5000L

3C5000L

3C5000L CPUCFG

CPUCFG CPUCFG rd, rj rj

rd

32 1 0 LA32

CPUCFG.1.LA32[bit0] 1 1

LA32 LA32 bit0 LA32

0 bitAA:BB

AA BB (AA-BB+1)

3C5000L “ ”

3C5000L

3C5000L

8- 1 3C5000L

0x0	31:0	PRId					32 ’ h14_c010
	1:0	ARCH	2'b00 LA32		2'b01 LA64		2 ’ b10
			LA32	2'b10		2'b11	
	2	PGMMU	1	MMU			1 ’ b1
	3	IOCSR	1	IOCSR			1 ’ b1
	11:4	PALEN			PALEN	1	8 ’ d47
	19:12	VALEN					

0x1

	17:15	LLFTP_ver	1	3 ' h1
	21	LSPW	1	1 ' b1
	22	LAM	1 AM*	1 ' b1
0x3	0	CCDMA	1 Cache Coherent DMA	1 ' b1
	1	SFB	1 Store Fill Buffer SFB	1 ' b1
	3	LLEXC	1 LL	1 ' b1
	4	SCDLY	1 SC	1 ' b1
	5	LLDBAR	1 LL dbar	1 ' b1
	6	ITLBHMC	1 ITLB TLB	1 ' b1
	7	ICHMC	1 ICache DCache	1 ' b1
	10:8	SPW_LVL	page walk	3 ' h4
	11	SPW_HP_HF	1 page walk TLB	1 ' b1
	12	RVA	1	1 ' b1
	16:13	RVMAX-1	-1	4 ' h7
0x4	31:0	CC_FREQ	Hz	N/A
0x5	15:0	CC_MUL		N/A
	31:16	CC_DIV		N/A
0x6	0	PMP	1	1 ' b1
	3:1	PMVER	1	3 ' h1
	7:4	PMNUM	-1	4 ' h3
	13:8	PMBITS	-1	6 ' h3f
	14	UPM	1	1 ' b1
0xa	0	L1 IU_Present	1 Cache Cache	1 ' b1
	1	L1 IU Unify	1 L1 IU_Present Cache Cache	1 ' b0
	2	L1 D Present	1 Cache	1 ' b1
	3	L2 IU Present	1 Cache Cache	1 ' b1
	4	L2 IU Unify	1 L2 IU_Present Cache Cache	1 ' b1
	5	L2 IU Private	1 L2 IU_Present Cache	1 ' b1
	6	L2 IU Inclusive	1 L2 IU_Present Cache L1	1 ' b0
	7	L2 D Present	1 Cache	1 ' b0
	8	L2 D Private	1 Cache	1 ' b0

	9	L2 D Inclusive	1 Cache L1	1'b0
	10	L3 IU Present	1 Cache Cache	1'b1
	11	L3 IU Unify	1 L3 IU_Present Cache Cache	1'b1
	12	L3 IU Private	1 L3 IU_Present Cache	1'b0
	13	L3 IU Inclusive	1 L3 IU_Present Cache L1 L2	1'b1
	14	L3 D Present	1 Cache	1'b0
	15	L3 D Private	1 Cache	1'b0
	16	L3 D Inclusive	1 Cache L1 L2	1'b0
0xb	15:0	Way-1	-1 10 L1 IU_Present Cache	16'h3
	23:16	Index-log2	log2(Cache) 10 L1 IU_Present Cache	8'h8
	30:24	Linesize-log2	log2(Cache) 10 L1 IU_Present Cache	8'h6
0xc	15:0	Way-1	-1 10 L1 D Present Cache	16'h3
	23:16	Index-log2	log2(Cache) 10 L1 D Present Cache	8'h8
	30:24	Linesize-log2	log2(Cache) 10 L1 D Present Cache	8'h6
0xd	15:0	Way-1	-1 10 L2 IU Present Cache	16'hf
	23:16	Index-log2	log2(Cache) 10 L2 IU Present Cache	8'h8
	30:24	Linesize-log2	log2(Cache) 10 L2 IU Present Cache	8'h6
0xe	15:0	Way-1	-1 10 L3 IU Present Cache	16'hf
	23:16	Index-log2	log2(Cache) 10 L3 IU Present Cache	8'h8
	30:24	Linesize-log2	log2(Cache) 10 L3 IU Present Cache	8'h6

8.2 3C5000L

3C5000L CSR

CSR JTAG

CSR IOCSRRD.B/H/W/D IOCSRWR.B/H/W/D

IOCSRRD.B/H/W/D IOCSRRD.B/H/W/D rd, rj rj

CSR CSR rd IOCSRWR.B/H/W/D

IOCSRWR.B/H/W/D rd, rj rj CSR

rd CSR IOCSRRD.B/H/W/D IOCSRWR.B/H/W/D

IOCSRRD.B/H/W/D IOCSRWR.B/H/W/D

0x1fe00000

9 Cache SCache

SCache 3C

Slock1_valid	0x0208	[63:63]	1
Slock1_addr	0x0208	[47:0]	1
Slock1_mask	0x0248	[47:0]	1
Slock2_valid	0x0210	[63:63]	2
Slock2_addr	0x0210	[47:0]	2
Slock2_mask	0x0250	[47:0]	2
Slock3_valid	0x0218	[63:63]	3
Slock3_addr	0x0218	[47:0]	3
Slock3_mask	0x0258	[47:0]	3

addr slock0_valid && ((addr & slock0_mask) == (slock0_addr & slock0_mask)) 1 0

4 scache 0x1fe00000 0x0280

9- 2 Cache SC_CONFIG

0	LRU en	RW	1'b1	Scache LRU
16	Prefetch En	RW	1'b1	Scache
22:20	Prefetch config	RW	3'h1	scache 0 – 4KB 1 – 16KB 2 – 64KB 3 – 1MB 7 – SCID_SEL==0
26:24	Prefetch lookahead	RW	3'h2	scache 0 – 1 – 0x100 2 – 0x200 3 – 0x300 4 – 0x400 5 – 0x500 6 – 0x600 7 – 0x700 SCID_SEL==0
30:28	Sc stall dirq cycle	RW	3'h2	SC dirq 0 – 1 cycle nonstall 1 – 16-31 cycle random 2 – 32-63 cycle random

				3- 64-127 cycle random 4 – 128-255 cycle random –
31	MCC storefill en	RW	1’b0	MCC storefill
34:32				
35	MCC clean exclusive replace en	RW	1’b0	
36	MCC clean shared replace en	RW	1’b0	

10

3C5000L 8 IPI BIOS

3C5000L 3A3000

10.1

3C5000L 0x3ff0_0000 0x1fe0_0000

0x3ff0_0000 disable_0x3ff0

10- 1 10- 5

10- 1

IPI_Status	R	32	1

INT4 ∧`

Core0_IPI_Enalbe	0x1004	RW	0	IPI_Enalbe
Core0_IPI_Set	0x1008	W	0	IPI_Set
Core0_IPI_Clear	0x100c	W	0	IPI_Clear
Core0_MailBox0	0x1020	RW	0	IPI_MailBox0
Core0_ MailBox1	0x1028	RW	0	IPI_MailBox1
Core0_ MailBox2	0x1030	RW	0	IPI_MailBox2
Core0_ MailBox3	0x1038	RW	0	IPI_MailBox3

10- 3 1

Core1_IPI_Status	0x1100	R	1	IPI_Status
Core1_IPI_Enalbe	0x1104	RW	1	IPI_Enalbe
Core1_IPI_Set	0x1108	W	1	IPI_Set
Core1_IPI_Clear	0x110c	W	1	IPI_Clear
Core1_MailBox0	0x1120	R	1	IPI_MailBox0
Core1_ MailBox1	0x1128	RW	1	IPI_MailBox1
Core1_ MailBox2	0x1130	W	1	IPI_MailBox2
Core1_ MailBox3	0x1138	W	1	IPI_MailBox3

10- 4 2

Core2_IPI_Status	0x1200	R	2	IPI_Status
Core2_IPI_Enalbe	0x1204	RW	2	IPI_Enalbe
Core2_IPI_Set	0x1208	W	2	IPI_Set
Core2_IPI_Clear	0x120c	W	2	IPI_Clear
Core2_MailBox0	0x1220	R	2	IPI_MailBox0
Core2_ MailBox1	0x1228	RW	2	IPI_MailBox1
Core2_ MailBox2	0x1230	W	2	IPI_MailBox2
Core2_ MailBox3	0x1238	W	2	IPI_MailBox3

10- 5 3

Core3_IPI_Status	0x1300	R	3	IPI_Status
Core3_IPI_Enalbe	0x1304	RW	3	IPI_Enalbe
Core3_IPI_Set	0x1308	W	3	IPI_Set
Core3_IPI_Clear	0x130c	W	3	IPI_Clear

Core3_MailBox0	0x1320	R	3	IPI_MailBox0
Core3_ MailBox1	0x1328	RW	3	IPI_MailBox1
Core3_ MailBox2	0x1330	W	3	IPI_MailBox2
Core3_ MailBox3	0x1338	W	3	IPI_MailBox3

3C5000L

3C5000L CC-NUMA

IPI

0 0 IPI_Status 0x1FE01000

1 0 0x10001FE01000

10.2

3C5000L

10- 6

perCore_IPI_Status	0x1000	R	IPI_Status
perCore_IPI_Enalbe	0x1004	RW	IPI_Enalbe
perCore_IPI_Set	0x1008	W	IPI_Set
perCore_IPI_Clear	0x100c	W	IPI_Clear
perCore_MailBox0	0x1020	RW	IPI_MailBox0
perCore_ MailBox1	0x1028	RW	IPI_MailBox1
perCore_ MailBox2	0x1030	RW	IPI_MailBox2
perCore_ MailBox3	0x1038	RW	IPI_MailBox3

MailBox

10- 7

IPI_Send	0x1040	WO	32 [31] 1 [30:26] [25:16] [15:5] [4:0] IPI_Status

Mail_Send	0x1048	WO	64 MailBox [63:32] MailBox [31] 1 [30:27] mask 32 1000b 0-2 0000b 0-3 [26] [25:16] [15:5] [4:2] MailBox 0 - MailBox0 32 1 - MailBox0 32 2 - MailBox1 32 3 - MailBox1 32 4 - MailBox2 32 5 - MailBox2 32 6 - MailBox3 32 7 - MailBox4 32 [1:0]
FREQ_Send	0x1058	WO	32 [31] 1 [30:27] mask 32 1000b 0-2 0000b 0-3 [26] [25:16] [15:5] [4:0] CSR[0x1050]

Mail_Send 32 64

Mail_Box

Mail_Box

10.3

IPI_Send Mail Send Freq Send Any Send

10- 8

ANY_Send	0x1158	WO	64 [63:32] [31] 1 [30:27] mask 32 1000b 0-2 0000b 0-3 [26] [25:16] [15:0]

11 I/O

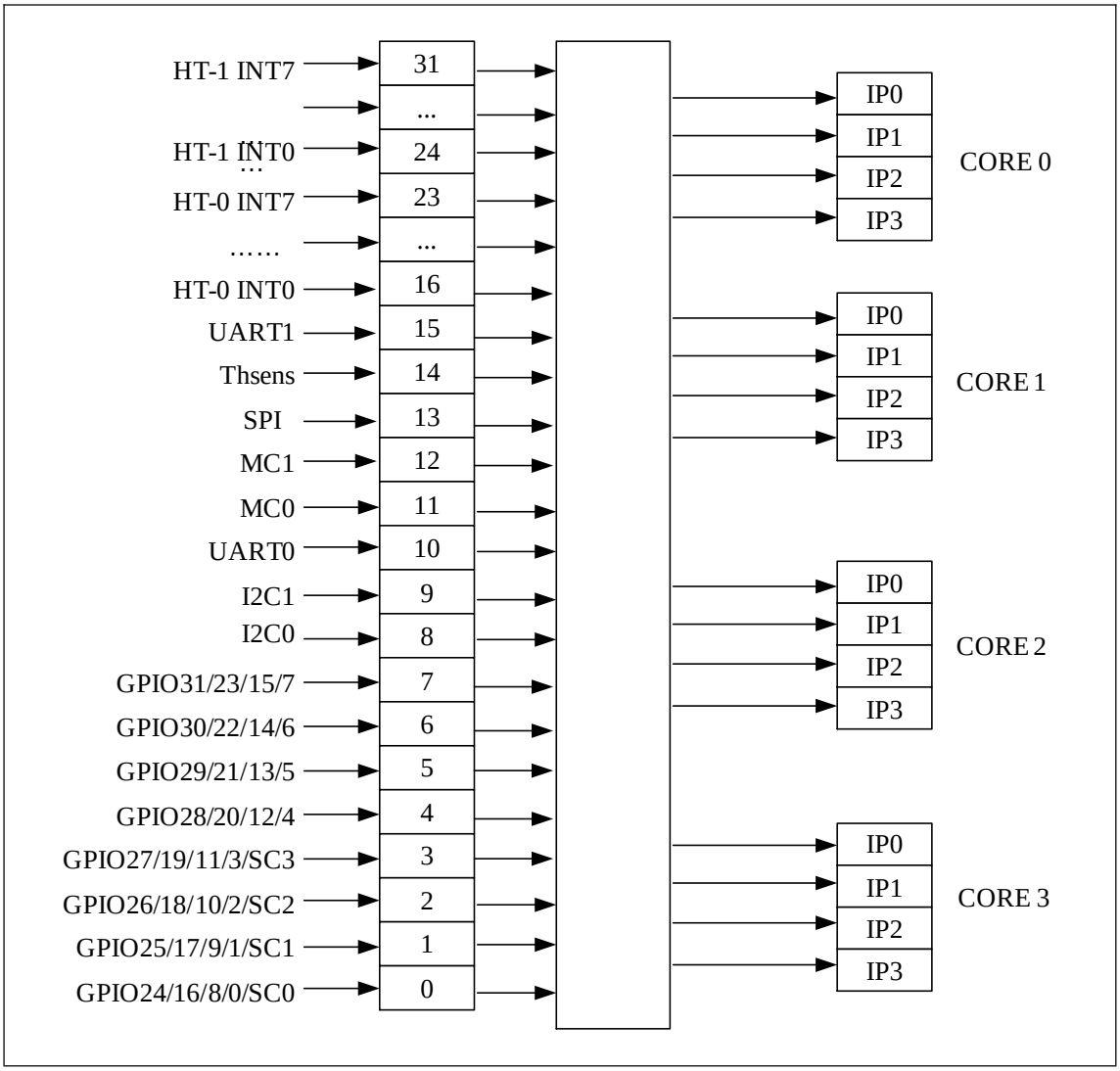
3C5000L 3A3000

IO HT

11.1 I/O

3C5000L 32

IO



11- 1 3C5000L

Enable Intenset Intenclr Inten Intenset
Intenset 1 Intenclr
Intenclr 1 Inten
Intedge 1 0
Intenclr

11- 1

	/				
	Intedge	Inten	Intenset	Intenclr	
0	RW / 0	R / 0	RW / 0	RW / 0	GPIO24/16/8/0/SC0
1	RW / 0	R / 0	RW / 0	RW / 0	GPIO25/17/9/1/SC1
2	RW / 0	R / 0	RW / 0	RW / 0	GPIO26/18/10/2/SC 2
3					

PC O

11.1.1

3A3000 0x1fe00000

0x3ff00000 0x3ff00000 disable_0x3ff0

11- 2 IO

Intisr	0x1420	32
Inten	0x1424	32
Intenset	0x1428	32
Intenclr	0x142c	32
Intedge	0x1434	32
CORE0_INTISR	0x1440	CORE0 32
CORE1_INTISR	0x1448	CORE1 32
CORE2_INTISR	0x1450	CORE2 32
CORE3_INTISR	0x1458	CORE3 32

3C5000L 4 32

INT0 INT3

CP0_Status IP2 IP5 32 I/O 8

11- 3 11- 4

0x48 3 INT2

3C5000L CSR[0x420][49]

[7:4] 0-7

0-7 0x28 3 INT2

11- 3

3:0	
7:4	

11- 4

Entry0	0x1400	GPIO24/16/8/0	Entry16	0x1410	HT0-int0

Entry1	0x1401	GPIO25/17/9/1	Entry17	0x1411	HT0-int1
Entry2	0x1402	GPIO26/18/10/2	Entry18	0x1412	HT0-int2
Entry3	0x1403	GPIO27/19/11/3	Entry19	0x1413	HT0-int3
Entry4	0x1404	GPIO28/20/12/4	Entry20	0x1414	HT0-int4
Entry5	0x1405	GPIO29/21/13/5	Entry21	0x1415	HT0-int5
Entry6	0x1406	GPIO30/22/14/6	Entry22	0x1416	HT0-int6
Entry7	0x1407	GPIO31/23/15/7	Entry23	0x1417	HT0-int7
Entry8	0x1408	I2C0	Entry24	0x1418	HT1-int0
Entry9	0x1409	I2C1	Entry25	0x1419	HT1-int1
Entry10	0x140a	UART0	Entry26	0x141a	HT1-int2
Entry11	0x140b	MC0	Entry27	0x141b	HT1-int3
Entry12	0x140c	MC1	Entry28	0x141c	HT1-int4
Entry13	0x140d	SPI	Entry29	0x141d	HT1-int5
Entry14	0x140e	Thsens	Entry30	0x141e	HT1-int6
Entry15	0x140f	UART1	Entry31	0x141f	HT1-int7

11.1.2

3C5000L

11- 5

perCore_INTISR	0x1010	32

11.2 I/O

I0 3C5000L I/0 HT

256 HT I0

IO “ ”

0x1fe00000 0x0420

11- 6

48	EXT_INT_en	RW	0x0	IO

IO HT

256

11.2.1

IO

0x1fe00000

11- 7 IO

EXT_IOIen[63:0]	0x1600	IO	[63:0]
EXT_IOIen[127:64]	0x1608	IO	[127:64]
EXT_IOIen[191:128]	0x1610	IO	[191:128]
EXT_IOIen[255:192]	0x1618	IO	[255:192]

11- 8 IO

EXT_IOIbounce[63:0]	0x1680	IO	[63:0]
EXT_IOIbounce[127:64]	0x1688	IO	[127:64]
EXT_IOIbounce[191:128]	0x1690	IO	[191:128]
EXT_IOIbounce[255:192]	0x1698	IO	[255:192]

11- 9 IO

EXT_IOIsr[63:0]	0x1700	IO	[63:0]
EXT_IOIsr[127:64]	0x1708	IO	[127:64]
EXT_IOIsr[191:128]	0x1710	IO	[191:128]
EXT_IOIsr[255:192]	0x1718	IO	[255:192]

11- 10 IO

CORE0_EXT_IOIsr[63:0]	0x1800	0	IO	[63:0]
CORE0_EXT_IOIsr[127:64]	0x1808	0	IO	[127:64]
CORE0_EXT_IOIsr[191:128]	0x1810	0	IO	[191:128]
CORE0_EXT_IOIsr[255:192]	0x1818	0	IO	[255:192]
CORE1_EXT_IOIsr[63:0]	0x1900	1	IO	[63:0]
CORE1_EXT_IOIsr[127:64]	0x1908	1	IO	[127:64]
CORE1_EXT_IOIsr[191:128]	0x1910	1	IO	[191:128]
CORE1_EXT_IOIsr[255:192]	0x1918	1	IO	[255:192]
CORE2_EXT_IOIsr[63:0]	0x1A00	2	IO	[63:0]
CORE2_EXT_IOIsr[127:64]	0x1A08	2	IO	[127:64]
CORE2_EXT_IOIsr[191:128]	0x1A10	2	IO	[191:128]
CORE2_EXT_IOIsr[255:192]	0x1A18	2	IO	[255:192]
CORE3_EXT_IOIsr[63:0]	0x1B00	3	IO	[63:0]
CORE3_EXT_IOIsr[127:64]	0x1B08	3	IO	[127:64]
CORE3_EXT_IOIsr[191:128]				

EXT_IOImap_Core255	0x1CFF	EXT_IOI[255]

11- 15

EXT_IOI_node_type0	0x14A0	16	0
EXT_IOI_node_type1	0x14A2	16	1
EXT_IOI_node_type2	0x14A4	16	2
……			
EXT_IOI_node_type15	0x14BE	16	15

11.2.2

11- 16 IO

perCore_EXT_IOIsr[63:0]	0x1800	IO e

11.2.4 IO HT

HT HT HT HT

256 256 4 8

HT IO

4

8

IO HT HT

256 4 8 256

IO HT

HT HT 0x90000efdfb000080

HT

IO IO 0x1800

12

12.1

3C5000L 0x1FE00198

0x1FE00000 0x0198

12- 1

24	Thsens0_overflow	R		0
25	Thsens1_overflow	R		1
47:32	Thsens0_out	R		0 =Thens0_out *731/0x4000 - 273 -40 – 125
65:48	Thsens1_out	R		1 =Thens1_out -*731/0x4000 - 273 -40 – 125

0x1FE00000

0x0428

12- 2 IO

Thsens_Temperature	0x0428	R	

12.2

4

GATE

Gate 0x198 16

EN 1

SEL 3C5000L

0 1

4

4

0x1fe00000

12- 3

Thsens_int_ctrl_Hi	0x1460	RW	[7:0] Hi_gate0 0 [8:8] Hi_en0 0 [11:10] Hi_Sel0 0 [23:16] Hi_gate1 1 [24:24] Hi_en1 1 [27:26] Hi_Sel1 1 [39:32] Hi_gate2 2 [40:40] Hi_en2 2 [43:42] Hi_Sel2 2 [55:48] Hi_gate3 3 [56:56] Hi_en3 3 [59:58] Hi_Sel3 3
Thsens_int_ctrl_Lo	0x1468	RW	[7:0] Lo_gate0 0 [8:8] Lo_en0 0 [11:10] Lo_Sel0 0 [23:16] Lo_gate1 1 [24:24] Lo_en1 1 [27:26] Lo_Sel1 1 [39:32] Lo_gate2 2 [40:40] Lo_en2 2 [43:42] Lo_Sel2 2 [55:48] Lo_gate3 3 [56:56] Lo_en3 3 [59:58] Lo_Sel3 3
Thsens_int_status/clr	0x1470	RW	1 [0] [1]

			[7:0] Hi_gate0 8 [15:8] Hi_gate1 8 [23:16] Hi_gate2 8 [31:24] Hi_gate3 8 [39:32] Lo_gate0 8 [47:40] Lo_gate1 8 [55:48] Lo_gate2 8
Thsens_int_up	0x1478	RW	[63:56] Lo_gate3 8

12.3

4

GATE

EN 1

SEL 3C5000L

FREQ FREQ

freqscale_mode_node

0x1fe00000

12- 4

Thsens_freq_scale	0x1480	RW	[7:0] Scale_gate0 0 [8:8] Scale_en0 0 [11:10] Scale_Sel0 0 [14:12] Scale_freq0 [23:16] Scale_gate1 1 [24:24] Scale_en1 1 [27:26] Scale_Sel1 1 [30:28] Scale_freq1 [39:32] Scale_gate2 2 [40:40] Scale_en2 2 [43:42] Scale_Sel2 2 [46:44] Scale_freq2 [55:48] Scale_gate3 3 [56:56] Scale_en3 3 [59:58] Scale_Sel3 3 [62:60] Scale_freq3
Thsens_freq_scale_up	0x1490	RW	[7:0] Scale_Hi_gate0 8 [15:8] Scale_Hi_gate1 8 [23:16] Scale_Hi_gate2 8 [31:24] Scale_Hi_gate3 8 [39:32] Scale_Lo_gate0 8 [47:40] Scale_Lo_gate1 8 [55:48] Scale_Lo_gate2 8 [63:56] Scale_Lo_gate3 8

12.4

PROCHOTn THERMTRIPn GPIO14 GPIO15 PROCHOTn THERMTRIPn

PROCHOTn

PROCHOTn 0

prochotn_freq_scale PROCHOTn

prochotn_o_sel 4

THERMTRIPn thermtripn_o_sel

4

THERMTRIPn PROCHOTn THERMTRIPn

PROCHOTn PROCHOTn

THERMTRIPn

12- 5

Thsens_hi_ctrl	0x1498	RW	[0:0] prochotn_oe PROCHOTn 0 1 [5:4] prochotn_o_sel PROCHOTn [10:8] prochotn_freq_scale PROCHOTn [17:16] thermtripn_o_sel THERMTRIPn

12.5

3C5000L 2

0x1FE00000

0x01580+vtsensor_id<<4

12- 6

0	Thsens_trigger	RW	0	thsens_mode thsens_cluster 0 temp_cluster
2	Thsens_mode	RW	0	0
3	Thsens_datarate	RW	0	0 – 10~20Hz 1 – 325~650Hz
6:4	Thsens_cluster	RW	0	0 1~7
8	Temp_valid	RW	0	CSR[0x198] Thsens0_out Thsens0_overflow

11:9	Temp_cluster	RW	0	Thsens_trigger

=data*731/0x4000 - 273 -40 ~ 125

12- 7

Cluster

13 DDR4 SDRAM

3C5000L DDR4 SDRAM JESD79-4

13.1 DDR4 SDRAM

3C5000L DDP 3DS DDP 8 CS 8 DDR4 SDRAM 4 3DS 4 CS 8 DDR4 SDRAM 32 RANK 22 18 2 Bank 2 Bank Group RASn CASn Wen

3C5000L DDR4 CS_n 8 RANK CHIP ID 8 ROW 18 COL 12 BANK 2 DDR4 BANK Group 2 CS_n Chip ID 13.4 CPU

3C5000L / / Slave State

3C5000L

- ，
- ，
- ，
- ， DCC
- ， ECC 1 2 1

- ， DDR4 SDRAM x4 x8 x16
- ， PHY 1/2
- ， 800Mbps-3200Mbps

13.2 DDR4 SDRAM

DDR4 SDRAM 13- 1 Command CMD RAS_n CAS_n WE_n 3 RAS_n=1, CAS_n=0, WE_n=1

TBD

13- 1 DDR4 SDRAM

Cas Latency CL = 5 Read Latency RL =5 Burst Length = 8

DDR4 SDRAM CMD ACT_n RAS_n CAS_n WE_n 4

ACT_n=1 RAS_n=1, CAS_n=0, WE_n=1

13.3 DDR4 SDRAM

DDR4 SDRAM TBD

13- 2 CMD RAS_n CAS_n WE_n 3

RAS_n=1, CAS_n=0, WE_n=0 DQM

DQM DQS

TBD

13- 2 DDR4 SDRAM

Cas Latency CL = 5 Wead Latency WL =5 Burst Length = 8

DDR4 SDRAM CMD ACT_n RAS_n CAS_n WE_n 4

ACT_n=1 RAS_n=1, CAS_n=0, WE_n=0

13.4 DDR4 SDRAM

13.4.1

13- 1

Offset	63:55	55:48	47:40	39:32	31:24	23:16	15:8	7:0
PHY								
0x0000							version(RD)	
0x0008			x4_mode	ddr3_mode			capability RD	
0x0010							dram_init(RD)	init_start
0x0018								
0x0020							preamble2	rdfifo_valid

0x0028		rdfifo_empty(RD)				Overflow(RD)		
0x0030		dll_value(RD)	dll_init_done(RD)	dll_lock_mode	dll_bypass	dll_adjj_cnt	dll_increment	dll_start_point
0x0038				dll_dbl_fix			dll_close_disable	dll_ck
0x0040				dbl_ctrl_ckca				dll_dbl_ckca
0x0048	pll_ctrl_ckca				pll_lock_ckca(RD)	dll_lock_ckca(RD)	clken_ckca	clksel_ckca
0x0050				dbl_ctrl_ds_0				dll_dbl_ds_0
0x0058	pll_ctrl_ds_0				pll_lock_ds_0(RD)	dll_lock_ds_0(RD)	clken_ds_0	clksel_ds_0
0x0060				dbl_ctrl_ds_1				dll_dbl_ds_1
0x0068	pll_ctrl_ds_1				pll_lock_ds_1(RD)	dll_lock_ds_1(RD)	clken_ds_1	clksel_ds_1
0x0070				dbl_ctrl_ds_2				dll_dbl_ds_2
0x0078	pll_ctrl_ds_2				pll_lock_ds_2(RD)	dll_lock_ds_2(RD)	clken_ds_2	clksel_ds_2
0x0080				dbl_ctrl_ds_3				dll_dbl_ds_3
0x0088	pll_ctrl_ds_3				pll_lock_ds_3(RD)	dll_lock_ds_3(RD)	clken_ds_3	clksel_ds_3
0x0090				dbl_ctrl_ds_4				dll_dbl_ds_4
0x0098	pll_ctrl_ds_4				pll_lock_ds_4(RD)	dll_lock_ds_4(RD)	clken_ds_4	clksel_ds_4
0x00a0				dbl_ctrl_ds_5				dll_dbl_ds_5
0x00a8	pll_ctrl_ds_5				pll_lock_ds_5(RD)	dll_lock_ds_5(RD)	clken_ds_5	clksel_ds_5
0x00b0				dbl_ctrl_ds_6				dll_dbl_ds_6
0x00b8	pll_ctrl_ds_6				pll_lock_ds_6(RD)	dll_lock_ds_6(RD)	clken_ds_6	clksel_ds_6
0x00c0				dbl_ctrl_ds_7				dll_dbl_ds_7
0x00c8	pll_ctrl_ds_7				pll_lock_ds_7(RD)	dll_lock_ds_7(RD)	clken_ds_7	clksel_ds_7
0x00d0				dbl_ctrl_ds_8				dll_dbl_ds_8
0x00d8	pll_ctrl_ds_8				pll_lock_ds_8(RD)	dll_lock_ds_8(RD)	clken_ds_8	clksel_ds_8
0x00e0			vrefclk_inv	vref_sample		vref_num	vref_dly	dll_vref
……								
0x0100					dll_1xdly_0	dll_1xgen_0	dll_wrdqs_0	dll_wrdq_0
0x0108						dll_gate_0	dll_rddqs1_0	dll_rddqs0_0
0x0110	rdodt_ctrl_0	rdgate_len_0	rdgate_mode_0	rdgate_ctrl_0			dqs_oe_ctrl_0	dq_oe_ctrl_0
0x0118						dly_2x_0	redge_sel_0	rddqs_phase_0(RD)
0x0120	w_bdly0_0[31:28]	w_bdly0_0[27:24]	w_bdly0_0[23:20]	w_bdly0_0[19:16]	w_bdly0_0[15:12]	w_bdly0_0[11:8]	w_bdly0_0[7:4]	w_bdly0_0[3:0]
0x0128		w_bdly0_0[59:56]	w_bdly0_0[55:52]	w_bdly0_0[51:48]	w_bdly0_0[47:44]	w_bdly0_0[43:40]	w_bdly0_0[39:36]	w_bdly0_0[35:32]
0x0130	w_bdly1_0[24:21]	w_bdly1_0[20:18]	w_bdly1_0[17:15]	w_bdly1_0[14:12]	w_bdly1_0[11:9]	w_bdly1_0[8:6]	w_bdly1_0[5:3]	w_bdly1_0[2:0]
0x0138								w_bdly1_0[27:26]
0x0140							rg_bdly_0[7:4]	rg_bdly_0[3:0]
0x0148								
0x0150	rdqsp_bdly_0[31:28]	rdqsp_bdly_0[27:24]	rdqsp_bdly_0[23:20]	rdqsp_bdly_0[19:16]	rdqsp_bdly_0[15:12]	rdqsp_bdly_0[11:8]	rdqsp_bdly_0[7:4]	rdqsp_bdly_0[3:0]
0x0158								rdqsp_bdly_0[35:32]
0x0160	rdqsn_bdly_0[31:28]	rdqsn_bdly_0[27:24]	rdqsn_bdly_0[23:20]	rdqsn_bdly_0[19:16]	rdqsn_bdly_0[15:12]	rdqsn_bdly_0[11:8]	rdqsn_bdly_0[7:4]	rdqsn_bdly_0[3:0]

0x0168								rdqsn_bdly_0[35:32]
0x0170	rdq_bdly_0[24:21]	rdq_bdly_0[20:18]	rdq_bdly_0[17:15]	rdq_bdly_0[14:12]	rdq_bdly_0[11:9]	rdq_bdly_0[8:6]	rdq_bdly_0[5:3]	rdq_bdly_0[2:0]
0x0178								rdq_bdly_0[27:26]
0x0180					dll_1xdly_1	dll_1xgen_1	dll_wrdqs_1	dll_wrdq_1
0x0188						dll_gate_1	dll_rddqs1_1	dll_rddqs0_1
0x0190	rdodt_ctrl_1	rdgate_len_1	rdgate_mode_1	rdgate_ctrl_1			dqs_oe_ctrl_1	dq_oe_ctrl_1
0x0198						dly_2x_1	redge_sel_1	rddqs_phase_1(RD)
0x01a0	w_bdly0_1[31:28]	w_bdly0_1[27:24]	w_bdly0_1[23:20]	w_bdly0_1[19:16]	w_bdly0_1[15:12]	w_bdly0_1[11:8]	w_bdly0_1[7:4]	w_bdly0_1[3:0]
0x01a8		w_bdly0_1[59:56]	w_bdly0_1[55:52]	w_bdly0_1[51:48]	w_bdly0_1[47:44]	w_bdly0_1[43:40]	w_bdly0_1[39:36]	w_bdly0_1[35:32]
0x01b0	w_bdly1_1[24:21]	w_bdly1_1[20:18]	w_bdly1_1[17:15]	w_bdly1_1[14:12]	w_bdly1_1[11:9]	w_bdly1_1[8:6]	w_bdly1_1[5:3]	w_bdly1_1[2:0]
0x01b8								w_bdly1_1[27:26]
0x01c0							rg_bdly_1[7:4]	rg_bdly_1[3:0]
0x01c8								
0x01d0	rdqsp_bdly_1[31:28]	rdqsp_bdly_1[27:24]	rdqsp_bdly_1[23:20]	rdqsp_bdly_1[19:16]	rdqsp_bdly_1[15:12]	rdqsp_bdly_1[11:8]	rdqsp_bdly_1[7:4]	rdqsp_bdly_1[3:0]
0x01d8								rdqsp_bdly_1[35:32]
0x01e0	rdqsn_bdly_1[31:28]	rdqsn_bdly_1[27:24]	rdqsn_bdly_1[23:20]	rdqsn_bdly_1[19:16]	rdqsn_bdly_1[15:12]	rdqsn_bdly_1[11:8]	rdqsn_bdly_1[7:4]	rdqsn_bdly_1[3:0]
0x01e8								rdqsn_bdly_1[35:32]
0x01f0	rdq_bdly_1[24:21]	rdq_bdly_1[20:18]	rdq_bdly_1[17:15]	rdq_bdly_1[14:12]	rdq_bdly_1[11:9]	rdq_bdly_1[8:6]	rdq_bdly_1[5:3]	rdq_bdly_1[2:0]
0x01f8								rdq_bdly_1[27:26]
0x0200					dll_1xdly_2	dll_1xgen_2	dll_wrdqs_2	dll_wrdq_2
0x0208						dll_gate_2	dll_rddqs1_2	dll_rddqs0_2
0x0210	rdodt_ctrl_2	rdgate_len_2	rdgate_mode_2	rdgate_ctrl_2			dqs_oe_ctrl_2	dq_oe_ctrl_2
0x0218						dly_2x_2	redge_sel_2	rddqs_phase_2(RD)
0x0220	w_bdly0_2[31:28]	w_bdly0_2[27:24]	w_bdly0_2[23:20]	w_bdly0_2[19:16]	w_bdly0_2[15:12]	w_bdly0_2[11:8]	w_bdly0_2[7:4]	w_bdly0_2[3:0]
0x0228		w_bdly0_2[59:56]	w_bdly0_2[55:52]	w_bdly0_2[51:48]	w_bdly0_2[47:44]	w_bdly0_2[43:40]	w_bdly0_2[39:36]	w_bdly0_2[35:32]
0x0230	w_bdly1_2[24:21]	w_bdly1_2[20:18]	w_bdly1_2[17:15]	w_bdly1_2[14:12]	w_bdly1_2[11:9]	w_bdly1_2[8:6]	w_bdly1_2[5:3]	w_bdly1_2[2:0]
0x0238								w_bdly1_2[27:26]
0x0240							rg_bdly_2[7:4]	rg_bdly_2[3:0]
0x0248								
0x0250	rdqsp_bdly_2[31:28]	rdqsp_bdly_2[27:24]	rdqsp_bdly_2[23:20]	rdqsp_bdly_2[19:16]	rdqsp_bdly_2[15:12]	rdqsp_bdly_2[11:8]	rdqsp_bdly_2[7:4]	rdqsp_bdly_2[3:0]
0x0258								rdqsp_bdly_2[35:32]
0x0260	rdqsn_bdly_2[31:28]	rdqsn_bdly_2[27:24]	rdqsn_bdly_2[23:20]	rdqsn_bdly_2[19:16]	rdqsn_bdly_2[15:12]	rdqsn_bdly_2[11:8]	rdqsn_bdly_2[7:4]	rdqsn_bdly_2[3:0]
0x0268								rdqsn_bdly_2[35:32]
0x0270	rdq_bdly_2[24:21]	rdq_bdly_2[20:18]	rdq_bdly_2[17:15]	rdq_bdly_2[14:12]	rdq_bdly_2[11:9]	rdq_bdly_2[8:6]	rdq_bdly_2[5:3]	rdq_bdly_2[2:0]
0x0278								rdq_bdly_2[27:26]
0x0280					dll_1xdly_3	dll_1xgen_3	dll_wrdqs_3	dll_wrdq_3

0x0288						dll_gate_3	dll_rddqs1_3	dll_rddqs0_3
0x0290	rdodt_ctrl_3	rdgate_len_3	rdgate_mode_3	rdgate_ctrl_3			dqs_oe_ctrl_3	dq_oe_ctrl_3
0x0298						dly_2x_3	redge_sel_3	rddqs_phase_3(RD)
0x02a0	w_bdly0_3[31:28]	w_bdly0_3[27:24]	w_bdly0_3[23:20]	w_bdly0_3[19:16]	w_bdly0_3[15:12]	w_bdly0_3[11:8]	w_bdly0_3[7:4]	w_bdly0_3[3:0]
0x02a8		w_bdly0_3[59:56]	w_bdly0_3[55:52]	w_bdly0_3[51:48]	w_bdly0_3[47:44]	w_bdly0_3[43:40]	w_bdly0_3[39:36]	w_bdly0_3[35:32]
0x02b0	w_bdly1_3[24:21]	w_bdly1_3[20:18]	w_bdly1_3[17:15]	w_bdly1_3[14:12]	w_bdly1_3[11:9]	w_bdly1_3[8:6]	w_bdly1_3[5:3]	w_bdly1_3[2:0]
0x02b8								w_bdly1_3[27:26]
0x02c0							rg_bdly_3[7:4]	rg_bdly_3[3:0]
0x02c8								
0x02d0	rdqsp_bdly_3[31:28]	rdqsp_bdly_3[27:24]	rdqsp_bdly_3[23:20]	rdqsp_bdly_3[19:16]	rdqsp_bdly_3[15:12]	rdqsp_bdly_3[11:8]	rdqsp_bdly_3[7:4]	rdqsp_bdly_3[3:0]
0x02d8								rdqsp_bdly_3[35:32]
0x02e0	rdqsn_bdly_3[31:28]	rdqsn_bdly_3[27:24]	rdqsn_bdly_3[23:20]	rdqsn_bdly_3[19:16]	rdqsn_bdly_3[15:12]	rdqsn_bdly_3[11:8]	rdqsn_bdly_3[7:4]	rdqsn_bdly_3[3:0]
0x02e8								rdqsn_bdly_3[35:32]
0x02f0	rdq_bdly_3[24:21]	rdq_bdly_3[20:18]	rdq_bdly_3[17:15]	rdq_bdly_3[14:12]	rdq_bdly_3[11:9]	rdq_bdly_3[8:6]	rdq_bdly_3[5:3]	rdq_bdly_3[2:0]
0x02f8								rdq_bdly_3[27:26]
0x0300					dll_1xdly_4	dll_1xgen_4	dll_wrdqs_4	dll_wrdq_4
0x0308						dll_gate_4	dll_rddqs1_4	dll_rddqs0_4
0x0310	rdodt_ctrl_4	rdgate_len_4	rdgate_mode_4	rdgate_ctrl_4			dqs_oe_ctrl_4	dq_oe_ctrl_4
0x0318						dly_2x_4	redge_sel_4	rddqs_phase_4(RD)
0x0320	w_bdly0_4[31:28]	w_bdly0_4[27:24]	w_bdly0_4[23:20]	w_bdly0_4[19:16]	w_bdly0_4[15:12]	w_bdly0_4[11:8]	w_bdly0_4[7:4]	w_bdly0_4[3:0]
0x0328		w_bdly0_4[59:56]	w_bdly0_4[55:52]	w_bdly0_4[51:48]	w_bdly0_4[47:44]	w_bdly0_4[43:40]	w_bdly0_4[39:36]	w_bdly0_4[35:32]
0x0330	w_bdly1_4[24:21]	w_bdly1_4[20:18]	w_bdly1_4[17:15]	w_bdly1_4[14:12]	w_bdly1_4[11:9]	w_bdly1_4[8:6]	w_bdly1_4[5:3]	w_bdly1_4[2:0]
0x0338								w_bdly1_4[27:26]
0x0340							rg_bdly_4[7:4]	rg_bdly_4[3:0]
0x0348								
0x0350	rdqsp_bdly_4[31:28]	rdqsp_bdly_4[27:24]	rdqsp_bdly_4[23:20]	rdqsp_bdly_4[19:16]	rdqsp_bdly_4[15:12]	rdqsp_bdly_4[11:8]	rdqsp_bdly_4[7:4]	rdqsp_bdly_4[3:0]
0x0358								rdqsp_bdly_4[35:32]
0x0360	rdqsn_bdly_4[31:28]	rdqsn_bdly_4[27:24]	rdqsn_bdly_4[23:20]	rdqsn_bdly_4[19:16]	rdqsn_bdly_4[15:12]	rdqsn_bdly_4[11:8]	rdqsn_bdly_4[7:4]	rdqsn_bdly_4[3:0]
0x0368								rdqsn_bdly_4[35:32]
0x0370	rdq_bdly_4[24:21]	rdq_bdly_4[20:18]	rdq_bdly_4[17:15]	rdq_bdly_4[14:12]	rdq_bdly_4[11:9]	rdq_bdly_4[8:6]	rdq_bdly_4[5:3]	rdq_bdly_4[2:0]
0x0378								rdq_bdly_4[27:26]
0x0380					dll_1xdly_5	dll_1xgen_5	dll_wrdqs_5	dll_wrdq_5
0x0388						dll_gate_5	dll_rddqs1_5	dll_rddqs0_5
0x0390	rdodt_ctrl_5	rdgate_len_5	rdgate_mode_5	rdgate_ctrl_5			dqs_oe_ctrl_5	dq_oe_ctrl_5
0x0398						dly_2x_5	redge_sel_5	rddqs_phase_5(RD)
0x03a0	w_bdly0_5[31:28]	w_bdly0_5[27:24]	w_bdly0_5[23:20]	w_bdly0_5[19:16]	w_bdly0_5[15:12]	w_bdly0_5[11:8]	w_bdly0_5[7:4]	w_bdly0_5[3:0]

0x03a8		w_bdly0_5[59:56]	w_bdly0_5[55:52]	w_bdly0_5[51:48]	w_bdly0_5[47:44]	w_bdly0_5[43:40]	w_bdly0_5[39:36]	w_bdly0_5[35:32]
0x03b0	w_bdly1_5[24:21]	w_bdly1_5[20:18]	w_bdly1_5[17:15]	w_bdly1_5[14:12]	w_bdly1_5[11:9]	w_bdly1_5[8:6]	w_bdly1_5[5:3]	w_bdly1_5[2:0]
0x03b8								w_bdly1_5[27:26]
0x03c0							rg_bdly_5[7:4]	rg_bdly_5[3:0]
0x03c8								
0x03d0	rdqsp_bdly_5[31:28]	rdqsp_bdly_5[27:24]	rdqsp_bdly_5[23:20]	rdqsp_bdly_5[19:16]	rdqsp_bdly_5[15:12]	rdqsp_bdly_5[11:8]	rdqsp_bdly_5[7:4]	rdqsp_bdly_5[3:0]
0x03d8								

0x04c8								
0x04d0	rdqsp_bdly_7[31:28]	rdqsp_bdly_7[27:24]	rdqsp_bdly_7[23:20]	rdqsp_bdly_7[19:16]	rdqsp_bdly_7[15:12]	rdqsp_bdly_7[11:8]	rdqsp_bdly_7[7:4]	rdqsp_bdly_7[3:0]
0x04d8								rdqsp_bdly_7[35:32]
0x04e0	rdqsn_bdly_7[31:28]	rdqsn_bdly_7[27:24]	rdqsn_bdly_7[23:20]	rdqsn_bdly_7[19:16]	rdqsn_bdly_7[15:12]	rdqsn_bdly_7[11:8]	rdqsn_bdly_7[7:4]	rdqsn_bdly_7[3:0]
0x04e8								rdqsn_bdly_7[35:32]
0x04f0	rdq_bdly_7[24:21]	rdq_bdly_7[20:18]	rdq_bdly_7[17:15]	rdq_bdly_7[14:12]	rdq_bdly_7[11:9]	rdq_bdly_7[8:6]	rdq_bdly_7[5:3]	rdq_bdly_7[2:0]
0x04f8								rdq_bdly_7[27:26]
0x0500					dll_1xdly_8	dll_1xgen_8	dll_wrdqs_8	dll_wrdq_8
0x0508						dll_gate_8	dll_rddqs1_8	dll_rddqs0_8
0x0510	rdodt_ctrl_8	rdgate_len_8	rdgate_mode_8	rdgate_ctrl_8			dqs_oe_ctrl_8	dq_oe_ctrl_8
0x0518						dly_2x_8	redge_sel_8	rddqs_phase_8(RD)
0x0520	w_bdly0_8[31:28]	w_bdly0_8[27:24]	w_bdly0_8[23:20]	w_bdly0_8[19:16]	w_bdly0_8[15:12]	w_bdly0_8[11:8]	w_bdly0_8[7:4]	w_bdly0_8[3:0]
0x0528		w_bdly0_8[59:56]	w_bdly0_8[55:52]	w_bdly0_8[51:48]	w_bdly0_8[47:44]	w_bdly0_8[43:40]	w_bdly0_8[39:36]	w_bdly0_8[35:32]
0x0530	w_bdly1_8[24:21]	w_bdly1_8[20:18]	w_bdly1_8[17:15]	w_bdly1_8[14:12]	w_bdly1_8[11:9]	w_bdly1_8[8:6]	w_bdly1_8[5:3]	w_bdly1_8[2:0]
0x0538								w_bdly1_8[27:26]
0x0540							rg_bdly_8[7:4]	rg_bdly_8[3:0]
0x0548								
0x0550	rdqsp_bdly_8[31:28]	rdqsp_bdly_8[27:24]	rdqsp_bdly_8[23:20]	rdqsp_bdly_8[19:16]	rdqsp_bdly_8[15:12]	rdqsp_bdly_8[11:8]	rdqsp_bdly_8[7:4]	rdqsp_bdly_8[3:0]
0x0558								rdqsp_bdly_8[35:32]
0x0560	rdqsn_bdly_8[31:28]	rdqsn_bdly_8[27:24]	rdqsn_bdly_8[23:20]	rdqsn_bdly_8[19:16]	rdqsn_bdly_8[15:12]	rdqsn_bdly_8[11:8]	rdqsn_bdly_8[7:4]	rdqsn_bdly_8[3:0]
0x0568								rdqsn_bdly_8[35:32]
0x0570	rdq_bdly_8[24:21]	rdq_bdly_8[20:18]	rdq_bdly_8[17:15]	rdq_bdly_8[14:12]	rdq_bdly_8[11:9]	rdq_bdly_8[8:6]	rdq_bdly_8[5:3]	rdq_bdly_8[2:0]
0x0578								rdq_bdly_8[27:26]
……								
0x0700					leveling_cs	tLVL_DELAY	leveling_req(WR)	leveling_mode
0x0708							leveling_done(RD)	leveling_ready(RD)
0x0710	leveling_resp_7	leveling_resp_6	leveling_resp_5	leveling_resp_4	leveling_resp_3	leveling_resp_2	leveling_resp_1	leveling_resp_0
0x0718								leveling_resp_8
0x0720								
……								
0x0800	dfe_ctrl_ds	pad_ctrl_ds				pad_ctrl_ck		
0x0808		pad_reset_po	pad_oplen_ca	pad_opdly_ca		pad_ctrl_ca		
0x0810	vref_ctrl_ds_3		vref_ctrl_ds_2		vref_ctrl_ds_1		vref_ctrl_ds_0	
0x0818	vref_ctrl_ds_7		vref_ctrl_ds_6		vref_ctrl_ds_5		vref_ctrl_ds_4	
0x0820							vref_ctrl_ds_8	
0x0828								

0x1188			mr_6_cs_0_ddr4		mr_5_cs_0_ddr4		mr_4_cs_0_ddr4	
0x1190	mr_3_cs_1_ddr4		mr_2_cs_1_ddr4		mr_1_cs_1_ddr4		mr_0_cs_1_ddr4	
0x1198			mr_6_cs_1_ddr4		mr_5_cs_1_ddr4		mr_4_cs_1_ddr4	
0x11a0	mr_3_cs_2_ddr4		mr_2_cs_2_ddr4		mr_1_cs_2_ddr4		mr_0_cs_2_ddr4	
0x11a8			mr_6_cs_2_ddr4		mr_5_cs_2_ddr4		mr_4_cs_2_ddr4	
0x11b0	mr_3_cs_3_ddr4		mr_2_cs_3_ddr4		mr_1_cs_3_ddr4		mr_0_cs_3_ddr4	
0x11b8			mr_6_cs_3_ddr4		mr_5_cs_3_ddr4		mr_4_cs_3_ddr4	
0x11c0	mr_3_cs_4_ddr4		mr_2_cs_4_ddr4		mr_1_cs_4_ddr4		mr_0_cs_4_ddr4	
0x11c8			mr_6_cs_4_ddr4		mr_5_cs_4_ddr4		mr_4_cs_4_ddr4	
0x11d0	mr_3_cs_5_ddr4		mr_2_cs_5_ddr4		mr_1_cs_5_ddr4		mr_0_cs_5_ddr4	
0x11d8			mr_6_cs_5_ddr4		mr_5_cs_5_ddr4		mr_4_cs_5_ddr4	
0x11e0	mr_3_cs_6_ddr4		mr_2_cs_6_ddr4		mr_1_cs_6_ddr4		mr_0_cs_6_ddr4	
0x11e8			mr_6_cs_6_ddr4		mr_5_cs_6_ddr4		mr_4_cs_6_ddr4	
0x11f0	mr_3_cs_7_ddr4		mr_2_cs_7_ddr4		mr_1_cs_7_ddr4		mr_0_cs_7_ddr4	
0x11f8			mr_6_cs_7_ddr4		mr_5_cs_7_ddr4		mr_4_cs_7_ddr4	
0x1200			nc16_map	nc	channel_width	ba_xor_row_offset	addr_new	cs_place
0x1208						bg_xor_row_offset		addr_mirror
0x1210	addr_base_1				addr_base_0			
0x1218								
0x1220	addr_mask_1				addr_mask_0			
0x1228								
0x1230			cs_diff	c_diff	bg_diff	ba_diff	row_diff	col_diff
0x1238				CF_confbus_timeout				
0x1240	WRQthreshold	tRDQidle	wr_pkc_num	rwq_rb	retry	no_dead_inorder	placement_en	stb_en/pbuf
0x1248								tRWGNTidle
0x1250							rfifo_age	
0x1258	prior_age3		prior_age2		prior_age1		prior_age0	
0x1260	retry_cnt(RD)					rbuffer_max(RD)	rdfifo_depth	stat_en
0x1268								
……								
0x1280	aw_512_align		rd_before_wr	ecc_enable		int_vector(RD)	int_trigger(RD)	int_enable
0x1288								
0x1290						int_cnt_fatal(RD)	int_cnt_err(RD)	int_cnt
0x1298	ecc_cnt_cs_7(RD)	ecc_cnt_cs_6(RD)	ecc_cnt_cs_5(RD)	ecc_cnt_cs_4(RD)	ecc_cnt_cs_3(RD)	ecc_cnt_cs_2(RD)	ecc_cnt_cs_1(RD)	ecc_cnt_cs_0(RD)
0x12a0	ecc_data_dir(RD)	ecc_code_dir(RD)	ecc_code_256(RD)					ecc_code_64(RD)
0x12a8	ecc_addr(RD)							
0x12b0	ecc_data[63:0](RD)							
0x12b8	ecc_data[127:64] (RD)							
0x12c0	ecc_data[191:128] (RD)							
0x12c8	ecc_data[255:192] (RD)							

……								
0x1300							ref_num	ref_sch_en
0x1308							Status_sref(RD)	srefresh_req
……								
0x1340	hardware_pd_7	hardware_pd_6	hardware_pd_5	hardware_pd_4	hardware_pd_3	hardware_pd_2	hardware_pd_1	hardware_pd_0
0x1348	power_sta_7(RD)	power_sta_6(RD)	power_sta_5(RD)	power_sta_4(RD)	power_sta_3(RD)	power_sta_2(RD)	power_sta_1(RD)	power_sta_0(RD)
0x1350	selfref_age		slowpd_age		fastpd_age		active_age	
0x1358				power_up				Age_step
0x1360	tCONF_IDLE				tLPMC_IDLE			
……								
0x1380								zq_overlap
0x1388								zq_stat_en
0x1390	zq_cnt_1(RD)				zq_cnt_0(RD)			
0x1398	zq_cnt_3(RD)				zq_cnt_2(RD)			
0x13a0	zq_cnt_5(RD)				zq_cnt_4(RD)			
0x13a8	zq_cnt_6(RD)				zq_cnt_6(RD)			
……								
0x13c0					odt_wr_cs_map			
0x13c8							odt_wr_length	odt_wr_delay
0x13d0					odt_rd_cs_map			
0x13d8							odt_rd_length	odt_rd_delay
……								
0x1400				tRESYNC_length	tRESYNC_delay	tRESYNC_shift	tRESYNC_max	tRESYNC_min
……								
0x1440					pre_predict		tm_cmdq_num	burst_length
0x1448								ca_timing
0x1450						wr/rd_dbi_en	ca_par_en	crc_en
0x1458							tCA_PAR	tWR_CRC
0x1460	bit_map_7	bit_map_6	bit_map_5	bit_map_6	bit_map_3	bit_map_2	bit_map_1	bit_map_0
0x1468	bit_map_15	bit_map_14	bit_map_13	bit_map_12	bit_map_11	bit_map_10	bit_map_9	bit_map_8
0x1470							bit_map_17	bit_map_16
0x1478								bitmap_mirror
0x1480				alertn_misc(RD)			alertn_cnt	alertn_clr
0x1488	alertn_addr(RD)							
……								
0x1500	win0_base							
0x1508	win1_base							
0x1510	win2_base							
0x1518	win3_base							
0x1520	win4_base							

0x1528	win5_base							
0x1530	win6_base							
0x1538	win7_base							
……								
0x1580	win0_mask							
0x1588	win1_mask							
0x1590	win2_mask							
0x1598	win3_mask							
0x15a0	win4_mask							
0x15a8	win5_mask							
0x15b0	win6_mask							
0x15b8	win7_mask							
……								
0x1600	win0_mmap							
0x1608	win1_mmap							
0x1610	win2_mmap							
0x1618	win3_mmap							
0x1620	win4_mmap							
0x1628	win5_mmap							
0x1630	win6_mmap							
0x1638	win7_mmap							
……								
0x1700							acc_hp	acc_en
0x1708	acc_fake_b				acc_fake_a			
0x1710								
0x1718								
0x1720	addr_base_acc_1				addr_base_acc_0			
0x1728								
0x1730	addr_mask_acc_1				addr_mask_acc_0			
0x1738								
MON								
0x2000								cmd_monitor
0x2008								
0x2010	cmd_fbck[63:0](RD)							
0x2018	cmd_fbck[127:64] (RD)							
0x2020					rw_switch_cnt(RD)			
……								
0x2100								scheduler_mon
0x2108								
0x2110	sch_cmd_num(RD)							

0x2118	ba_conflict_all(RD)							
0x2120	ba_conflict_last1(RD)							
0x2128	ba_conflict_last2(RD)							
0x2130	ba_conflict_last3(RD)							
0x2138	ba_conflict_last4(RD)							
0x2140	ba_conflict_last5(RD)							
0x2148	ba_conflict_last6(RD)							
0x2150	ba_conflict_last7(RD)							
0x2158	ba_conflict_last8(RD)							
0x2160	rd_conflict(RD)							
0x2168	wr_conflict(RD)							
0x2170	rtw_conflict(RD)							
0x2178	wtr_conflict(RD)							
0x2180	rd_conflict_last1(RD)							
0x2188	wr_conflict_last1(RD)							
0x2190	rtw_conflict_last1(RD)							
0x2198	wtr_conflict_last1(RD)							
0x21a0	wr_rd_turnaround(RD)							
0x21a8	cs_turnaround(RD)							
0x21b0	bg_conflict(RD)							
……								
0x2300						sm_leveling		sm_init
0x2308								
0x2310		sm_rank_03		sm_rank_02		sm_rank_01		sm_rank_00
0x2318		sm_rank_07		sm_rank_06		sm_rank_05		sm_rank_04
0x2320		sm_rank_11		sm_rank_10		sm_rank_09		sm_rank_08
0x2328		sm_rank_15		sm_rank_14		sm_rank_13		sm_rank_12
0x2330		sm_rank_19		sm_rank_18		sm_rank_17		sm_rank_16
0x2338		sm_rank_23		sm_rank_22		sm_rank_21		sm_rank_20
0x2340		sm_rank_27		sm_rank_26		sm_rank_25		sm_rank_24
0x2348		sm_rank_31		sm_rank_30		sm_rank_29		sm_rank_28
……								
TST								
0x3000						lpbk_mode	lpbk_start	lpbk_en
0x3008	lpbk_correct(RD)				lpbk_counter(RD)			lpbk_error(RD)
0x3010	lpbk_data_en[63:0]							
0x3018								lpbk_data_en[71:64]
0x3020							lpbk_data_mask_en	
0x3028								
0x3030	Lpbk_dat_w0[63:0]							

0x3038	Lpbk_dat_w0[127:64]							
0x3040	Lpbk_dat_w1[63:0]							
0x3048	Lpbk_dat_w1[127:64]							
0x3050		lpbk_ecc_mask_w0	lpbk_dat_mask_w0			lpbk_ecc_w0		
0x3058		lpbk_ecc_mask_w1	lpbk_dat_mask_w1			lpbk_ecc_w1		
0x3060								prbs_23
0x3068						prbs_init		
……								
0x3100					fix_data_pattern_index	bus_width	page_size	test_engine_en
0x3108			cs_diff_tst	c_diff_tst	bg_diff_tst	ba_diff_tst	row_diff_tst	col_diff_tst
0x3120	addr_base_tst							
0x3128								
0x3130	user_data_pattern							
0x3138								
0x3140	valid_bits[63:0]							
0x3148								valid_bits[71:64]
0x3150	ctrl[63:0]							
0x3158	ctrl[127:64]							
0x3160	obs[63:0] (RD)							
0x3168	obs[127:64] (RD)							
0x3170	obs[191:128] (RD)							
0x3178	obs[255:192] (RD)							
0x3180	obs[319:256] (RD)							
0x3188	obs[383:320] (RD)							
0x3190	obs[447:384] (RD)							
0x3198	obs[511:448] (RD)							
0x31a0	obs[575:512] (RD)							
0x31a8	obs[639:576] (RD)							
0x31b0					obs[671:640](RD)			
……								
0x3200								
0x3208								
0x3220	tud_i0							
0x3228	tud_i1							
0x3230	tud_o(RD)							
……								
0x3300	tst_300							

0x3308	tst_308
0x3310	tst_310
0x3318	tst_318
0x3320	tst_320
0x3328	tst_328
0x3330	tst_330
0x3338	tst_338
0x3340	tst_340
0x3348	tst_348
0x3350	tst_350
0x3358	tst_358
0x3360	tst_360
0x3368	tst_368
0x3370	tst_370
0x3378	tst_378

13.5

13.5.1

Init_start 0x010 0x2 Init_start

DRAM

(1) pm_clk_sel_ckca pm_clk_sel_ds

(2) pm_phy_init_start 1 PHY

(3) DLL pm_dll_init_done 1

(4) pm_dll_lock_* pm_pll_lock_* 1

(5) pm_clken_*

(6) pm_init_start 1

(7) pm_dram_init pm_cs_enable

13.5.2

STR pad_reset_po 0x808

DDR_RESETn

(1) reset_ctrl[1:0] == 2 ' b00

DDR_RESETn

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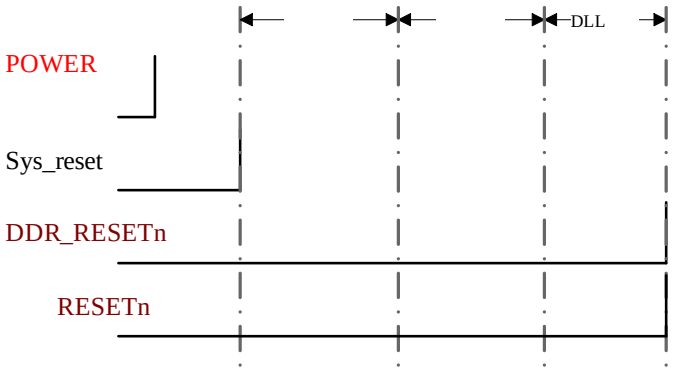

(2) reset_ctrl[1:0] == 2 ' b10

DDR_RESETn

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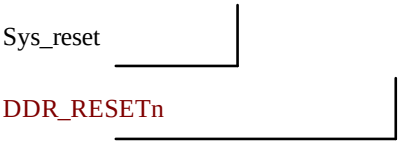

Sys_reset
DDR_RESETn

GATE DQ DQ

bit-deskew dataslice bit

13.5.3.1 Write Leveling

Write Leveling DQS

(1)

(2) Dll_wrdqs_x x = 0...8 0x20

(3) Dll_wrdq_x x = 0...8 0x0

(4) Lvl_mode 2'b01

(5) Lvl_ready 1 Write Leveling

(6) Lvl_req 1

(7) Lvl_done 1 Write Leveling

(8) Lvl_resp_x 0 Dll_wrdq_x[6:0] dll_1xdly[6:0] 1 5-7 Lvl_resp_x 1 9 1 Dll_wrdq_x[6:0] dll_1xdly[6:0] 1 5-7 Lvl_resp_x 0 Dll_wrdq_x[6:0] dll_1xdly[6:0] 1 5-7 Lvl_resp_x 1 9

(9) Dll_wrdq_x dll_1xdly 0x40 Dll_wrdq_x dll_1xdly

(10) DIMM pm_dly_2x 0x0 pm_dly_2x 0x010101

(11) Lvl_mode 0x700 2'b00 Write Leveling

13.5.3.2 Gate Leveling

Gate Leveling DQS

(1)

(2) Write Leveling

(3) Dll_gate_x x = 0...8 0

(4) Lvl_mode 2'b10

(5) Lvl_ready 1 Gate Leveling

(6) Lvl_req 1

(7) Lvl_done 1 Gate Leveling

(8) Lvl_resp_x[0] Lvl_resp_x[0] 1 Dll_gate_x[6:0] 1 6-8 0

(9) 0 Dll_gate_x[6:0] 1 6-9
1 Gate Leveling
(10) pm_rddqs_phase pm_rdedge_sel
(11) Dll_gate_x x = 0...8 0x20
(12) Lvl_req Lvl_resp_x[7:5]
Lvl_resp_x[4:2] Burst_length/2 13
4 Rd_oe_begin_x
Burst_length/2 Dll_gate_x
(13) Lvl_mode 0x700 2'b00 Gate Leveling
(14) Gate Leveling

13.5.4

pm_pad_ctrl_ca[0] 1

pm_pad_ctrl_ca[0] 0 DDR4 CAL Mode

13.5.5 MRS

(4) Mrs_req 0x1126 1 DRAM MRS

(5) Mrs_done 0x1127 1 MRS

0

(6) Command_mode 0x1120 0

13.5.6

DRAM Cmd_cs

Cmd_cmd Cmd_ba Cmd_a 0x1128 DRAM

(1) Cmd_cs Cmd_cmd Cmd_ba Cmd_a 0x1128

(2) Command_mode 0x1120 1

(3) Status_cmd 0x1122 1

0

(4) Cmd_req 0x1121 1 DRAM

(5) Command_mode 0x1120 0

13.5.7

test_phy test_phy

test_* test_phy

pm_*

(1)

(2)

(3) Lpbk_en 1

(4) Lpbk_start 1

(5)

(6) Lpbk_error 1
Lpbk_*
0

13.5.8 ECC

ECC 64

Ecc_enable 0x1280 2

Ecc_enable[0] ECC ECC

Ecc_enable[1] ECC

ECC Int_enable
Int_vector[0] ECC 1 2
Int_vecotr[1] ECC Int_vector 1

13.5.9

0 ECC Mc0_ecc_cnt	0x0610	RW	0 ECC [7:0]: MC0 int_cnt ECC [15:8]: MC0 int_cnt_err(RO) ECC [23:16]: MC0 int_cnt_fatal(RO) ECC
0 ECC Mc0_ecc_cs_cnt	0x0618	RO	0 ECC [7:0]: MC0 ecc_cnt_cs_0 CS0 ECC [15:8]: MC0 ecc_cnt_cs_1 CS1 ECC [23:16]: MC0 ecc_cnt_cs_2 CS2 ECC [31:24]: MC0 ecc_cnt_cs_3 CS3 ECC [39:32]: MC0 ecc_cnt_cs_4 CS4 ECC [47:40]: MC0 ecc_cnt_cs_5 CS5 ECC [55:48]: MC0 ecc_cnt_cs_6 CS6 ECC [63:56]: MC0 ecc_cnt_cs_7 CS7 ECC
0 ECC Mc0_ecc_code	0x0620	RO	0 ECC [7:0]: MC0 ecc_code_64 64 ECC ECC [41:32]: MC0 ecc_code_256 256 ECC ECC [52:48]: MC0 ecc_code_dir ECC [60:56]: MC0 ecc_data_dir ECC
0 ECC Mc0_ecc_addr	0x0628	RO	0 ECC [63:0]: MC0 ecc_addr ECC
0 ECC 0 Mc0_ecc_data0	0x0630	RO	0 ECC 0 [63:0]:Mc0_ecc_data0 ECC 64 ECC 256 ECC [63:0]
0 ECC 1 Mc0_ecc_data1	0x0638	RO	0 ECC 1 [63:0]:Mc0_ecc_data1 ECC 256 ECC [127:64]
0 ECC 2 Mc0_ecc_data2	0x0640	RO	0 ECC 2 [63:0]:Mc0_ecc_data2 ECC 256 ECC [191:128]
0 ECC 3 Mc0_ecc_data3	0x0648	RO	0 ECC 3 [63:0]:Mc0_ecc_data3 ECC 256 ECC [255:192]

13- 3 1

1 ECC Mc1_ecc_set	0x0700	RW	1 ECC [5:0] MC1 int_enable [8]: MC1 int_trigger [21:16]: MC1 int_vector(RO) [33:32]: MC1 ecc_enable ECC [40]: MC1 rd_before_wr
	0x0708	RW	
1 ECC Mc1_ecc_cnt	0x0710	RW	1 ECC [7:0]: MC1 int_cnt ECC [15:8]: MC1 int_cnt_err(RO) ECC [23:16]: MC1 int_cnt_fatal(RO) ECC
1 ECC Mc1_ecc_cs_cnt	0x0718	RO	1 ECC [7:0]: MC1 ecc_cnt_cs_0 CS0 ECC [15:8]: MC1 ecc_cnt_cs_1 CS1 ECC [23:16]: MC1 ecc_cnt_cs_2 CS2 ECC [31:24]: MC1 ecc_cnt_cs_3 CS3 ECC [39:32]: MC1 ecc_cnt_cs_4 CS4 ECC [47:40]: MC1 ecc_cnt_cs_5 CS5 ECC [55:48]: MC1 ecc_cnt_cs_6 CS6 ECC [63:56]: MC1 ecc_cnt_cs_7 CS7 ECC
1 ECC Mc1_ecc_code	0x0720	RO	1 ECC [7:0]: MC1 ecc_code_64 64 ECC ECC [41:32]: MC1 ecc_code_256 256 ECC ECC [52:48]: MC1 ecc_code_dir ECC [60:56]: MC1 ecc_data_dir ECC
1 ECC Mc1_ecc_addr	0x0728	RO	1 ECC [63:0]: MC1 ecc_addr ECC
1 ECC 0 Mc1_ecc_data0	0x0730	RO	1 ECC 0 [63:0]:Mc1_ecc_data0 ECC 64 ECC 256 ECC [63:0]

1 ECC 1 Mc1_ecc_data1	0x0738	RO	1 ECC 1 [63:0]:Mc1_ecc_data1 ECC ECC [127:64] 256
1 ECC 2 Mc1_ecc_data2	0x0740	RO	1 ECC 2 [63:0]:Mc1_ecc_data2 ECC ECC [191:128] 256
1 ECC 3 Mc1_ecc_data3	0x0748	RO	1 ECC 3 [63:0]:Mc1_ecc_data3 ECC ECC [255:192] 256

14 HyperTransport

3C5000L HyperTransport

HyperTransport

IO Cache

Uncache 14.5.14 Cache IO

DMA Cache ,

Cache HyperTransport HT0

(0x0C00_0000_0000 – 0x0DFF_FFFF_FFFF) Cache

HT1 (0x0E00_0000_0000 – 0x0FFF_FFFF_FFFF)

Cache

14.1

HT 3C5000L HT

8 8

3C5000L HyperTransport

- HT1.0/HT3.0
- 200/400/800/1600/2000/2400/3200MHz
- HT1.0 8
- HT3.0 8
- PowerOK Rstn LDT_Stopn
- DMA Cache/Uncache
- Cache

14.1 HyperTransport

HyperTransport ,

HyperTransport

14- 1 HyperTransport

HT0_8x2		1 16 HyperTransport 8 HT0_Lo address[40] = 0 HT0_Hi address[40] = 1; 1
HT0_Lo_mode		1 HT0_Lo HT0_Lo HT0_Lo_Powerok HT0_Lo_Rstn HT0_Lo_Ldt_Stopn “Act as Slave” 0 HyperTransport Bridge 1 0 0 HyperTransport P2P 1 0 HT0_Lo HT0_Lo_Powerok HT0_Lo_Rstn HT0_Lo_Ldt_Stopn HT
HT0_Lo_Powerok	Powerok	HyperTransport Powerok HT0_Lo_Mode 1 HT0_Lo HT0_Lo_Mode 0
HT0_Lo_Rstn	Rstn	HyperTransport Rstn HT0_Lo_Mode 1 HT0_Lo HT0_Lo_Mode 0
HT0_Lo_Ldt_Stopn	Ldt_Stopn	HyperTransport Ldt_Stopn HT0_Lo_Mode 1 HT0_Lo HT0_Lo_Mode 0
HT0_Lo_Ldt_Reqn	Ldt_Reqn	HyperTransport Ldt_Reqn
HT0_Hi_mode		
HT0_Hi_Powerok	Powerok	
HT0_Hi_Rstn	Rstn	
HT0_Hi_Ldt_Stopn	Ldt_Stopn	
HT0_Hi_Ldt_Reqn	Ldt_Reqn	
HT0_Rx_CLKp[1:0] HT0_Rx_CLKn[1:0] HT0_Tx_CLKp[1:0] HT0_Tx_CLKp[1:0]	CLK[1:0]	HyperTransport CLK
HT0_Rx_CTLp[1:0] HT0_Rx_CTLn[1:0] HT0_Tx_CTLp[1:0] HT0_Tx_CTLn[1:0]	CTL[1:0]	HyperTransport CTL

HT0_Rx_CADp[15:0] HT0_Rx_CADn[15:0] HT0_Tx_CADp[15:0] HT0_Tx_CADn[15:0]	CAD[15:0]	HyperTransport CAD [15:8]

HyperTransport HyperTransport

(200MHz) (8bit)

“Init Complete” 14.5.2

“Link Width Out” “Link Width In” 14.5.2

“Link Width Out” “Link Width In” “Link Freq”

“HT_Ldt_Stopn”

HyperTransport HyperTransport

HyperTransport

14.2 HyperTransport

3C5000L HyperTransport 1.03/3.0

HyperTransport HyperTransport

14- 2 HyperTransport

000000	-	NOP		
000001	NPC	FLUSH		
x01xxx	NPC or PC	Write	bit 5 0 - Nonposted 1 - Posted bit 2 0 – Byte 1 – Doubleword bit 1 Don’t Care bit 0 Don’t Care	bit 5 1 POSTED bit 2 0 – Byte 1 – Doubleword bit 1 Don’t Care bit 0 1
01xxxx	NPC	Read	bit 3 Don’t Care bit 2 0 – Byte 1 – Doubleword bit 1 Don’t Care bit 0 Don’t Care	bit 3 Don’t Care bit 2 0 – Byte 1 – Doubleword bit 1 Don’t Care bit 0 1
110000	R	RdResponse		
110011	R	TgtDone		
110100	PC	WrCoherent	----	
110101	PC	WrAddr	----	

111000	R	RespCoherent	----	
111001	NPC	RdCoherent	----	
111010	PC	Broadcast		
111011	NPC	RdAddr	----	
111100	PC	FENCE		
111111	-	Sync/Error	Sync/Error	

14- 3

000000	-	NOP		
x01x0x	NPC or PC	Write	bit 5 0 - Nonposted 1 - Posted bit 2 0 – Byte 1 – Doubleword bit 0 0	bit 5 1 POSTED bit 2 0 – Byte 1 – Doubleword bit 0 1
010x0x	NPC	Read	bit 2 0 – Byte 1 – Doubleword bit 0 Don't Care	bit 2 0 – Byte 1 – Doubleword bit 0 1
110000	R	RdResponse		
110011	R	TgtDone		
110100	PC	WrCoherent	----	
110101	PC	WrAddr	----	
111000	R	RespCoherent	----	
111001	NPC	RdCoherent	----	
111011	NPC	RdAddr	----	
111111	-	Sync/Error		

14.3 HyperTransport

HyperTransport 256 Fix Arbiter

EOI

14.5.7

14.3.1 PIC

PIC

PIC PIC PIC

PIC PIC PIC

4 PIC

3C5000L HyperTransport 3 PIC

256 4

PIC

14.3.2

HT

HT HT

CPU

HT

HT 0x90000efdfb000080

HT

14.3.3

3C5000L IO

HT PIC

IO HT IO

0x1800

HT 14.5.34

HT_int_trans =

14.4 HyperTransport

14.4.1 HyperTransport

3C5000L 4 HyperTransport

14- 5 4 HyperTransport

0x0A00_0000_0000	0x0AFF_FFFF_FFFF	1 Tbytes	HT0_LO
0x0B00_0000_0000	0x0BFF_FFFF_FFFF	1 Tbytes	HT0_HI
0x0E00_0000_0000	0x0EFF_FFFF_FFFF	1 Tbytes	HT1_LO
0x0F00_0000_0000	0x0FFF_FFFF_FFFF	1 Tbytes	HT1_HI

14.5.10	3	HyperTransport	HyperTransport	act_as_slave 0 P2P HyperTransport act_as_slave 1
Post 14.5.12	2		HyperTransport Post Write	Post Write Post Write HyperTransport
14.5.13	2		Cache	IO HT HyperTransport HyperTransport
Uncache 14.5.14	2	HyperTransport	HyperTransport Uncache	3C5000L IO DMA Cache SCache IO Uncache IO

14.5

AXI SLAVE HT RECEIVER

HT

HT 0xFD_FB00_0000 0xFD_FBFF_FFFF HT

Enable	0x00	Device ID		Vendor ID	
	0x04	Status		Command	
	0x08	Class Code			Revision ID
	0x0c	BIST	Header Type	Latency Timer	Cache Line Size

	0x10				
	0x14				
	0x18				
	0x1c				
	0x20				
	0x24				
	0x28	Cardbus CIS Pointer			
	0x2c	Subsystem ID		Subsystem Vendor ID	
	0x30	Expansion ROM Enable Address			
	0x34	Reserved			Capabilities Pointer
	0x38	Reserved			
	0x3c	Bridge Control		Interrupt Pin	Interrupt Line
Cap 0 PRI	0x40	Command		Capabilities Pointer	Capability ID
	0x44	Link Config 0		Link Control 0	
	0x48	Link Config 1		Link Control 1	
	0x4C	LinkFreqCap0		Link Error0/Link Freq 0	Revision ID
	0x50	LinkFreqCap1		Link Error1/Link Freq 1	Feature
	0x54	Error Handling		Enumeration Scratchpad	
	0x58	Reserved		Mem Limit Upper	Mem Enable Upper
Cap 1 Retry	0x60	Capability Type	Reserved	Capability Pointer	Capabiliter ID
	0x64	Status 1	Control 1	Status 0	Control 0
	0x68	Retry Count 1		Retry Count 0	
CAP 3	0x6C	Capability Type	Revision ID	Capability Pointer	Capabiliter ID
CAP 4 Interrupt	0x70	Capability Type	Index	Capability Pointer	Capabiliter ID
	0x74	Dataport			
	0x78	IntrInfo[31:0]			
	0x7C	IntrInfo[63:32]			
Int Vector	0x80	INT Vector[31:0]			
	0x84	INT Vector[63:32]			
	0x88	INT Vector[95:64]			
	0x8C	INT Vector[127:96]			
	0x90	INT Vector[159:128]			
	0x94	INT Vector[191:160]			
	0x98	INT Vector[223:192]			

	0x9C	INT Vector[255:224]			
	0xA0	INT Enable[31:0]			
	0xA4	INT Enable[63:32]			
	0xA8	INT Enable[95:64]			
	0xAC	INT Enable[127:96]			
	0xB0	INT Enable[159:128]			
	0xB4	INT Enable[191:160]			
	0xB8	INT Enable[223:192]			
	0xBC	INT Enable[255:224]			
CAP 5 Gen3	0xC0	Capability Type	Cap Enum/Index	Capability Pointer	Capabiliter ID
	0xC4	Global Link Training			
	0xC8	Transmitter Configuration 0			
	0xCC	Receiver Configuration 0			
	0xD0	Link Training 0			
	0xD4	Frequency Extension			
	0xD8	Transmitter Configuration 1			
	0xDC	Receiver Configuration 1			
	0xE0	Link Training 1			
	0xE4	BIST Control			

Enable	0x100	Device ID	Vendor ID		
	0x104	Status	Command		
	0x108	Class Code		Revision ID	
	0x10c	BIST	Header Type	Latency Timer	Cache Line Size
	0x110				
	0x114				
	0x118				
	0x11c				
	0x120				
	0x124				
	0x128	Cardbus CIS Pointer			
	0x12c	Subsystem ID	Subsystem Vendor ID		
	0x130	Expansion ROM Enable Address			
	0x134	Reserved		Capabilities Pointer	
	0x138	Reserved			
	0x13c	Bridge Control	Interrupt Pin	Interrupt Line	
Receive	0x140	HT RX Enable 0			

Windows	0x144	HT RX Mask 0
	0x148	HT RX Enable 1
	0x14C	HT RX Mask 1
	0x150	HT RX Enable 2
	0x154	HT RX Mask 2
	0x158	HT RX Enable 3
	0x15C	HT RX Mask 3
	0x160	HT RX Enable 4
	0x164	HT RX Mask 4
Header Trans	0x168	HT RX Header Trans
	0x16C	HT RX EXT Header Trans
Post Windows	0x170	HT TX Post Enable 0
	0x174	HT TX Post Mask 0
	0x178	HT TX Post Enable 1
	0x17C	HT TX Post Mask 1
Prefetchable Windows	0x180	HT TX Prefetchable Enable 0
	0x184	HT TX Prefetchable Mask 0
	0x188	HT TX Prefetchable Enable 1
	0x18C	HT TX Prefetchable Mask 1
Uncache Windows	0x190	HT RX Uncache Enable 0
	0x194	HT RX Uncache Mask 0
	0x198	HT RX Uncache Enable 1
	0x19C	HT RX Uncache Mask 1
	0x1A0	HT RX Uncache Enable 2
	0x1A4	HT RX Uncache Mask 2
	0x1A8	HT RX Uncache Enable 3
	0x1AC	HT RX Uncache Mask 3
P2P Windows	0x1B0	HT RX P2P Enable 0
	0x1B4	HT RX P2P Mask 0
	0x1B8	HT RX P2P Enable 1
	0x1BC	HT RX P2P Mask 1
APP Config	0x1C0	APP Configuration 0
	0x1C4	APP Configuration 1
	0x1C8	RX Bus Value
	0x1CC	PHY status
Buffer	0x1D0	TX Buffer 0
	0x1D4	TX Buffer 1 / Rx buffer hi
	0x1D8	TX Buffer turning

21:0	Reserved	22	0x0		

14.5.2 Capability Registers

0x40

0x20010008

Command Capabilities Pointer Capability ID

14- 9 Command Capabilities Pointer Capability ID

31:29	Slave/Pri	3	0x0	R	Command HOST/Sec
28:26	Reserved	2	0x0	R	
25:21	Unit Count	5	0x0	R/W	Unit
20:16	Unit ID	5	0x0		HOST ID SLAVE Unit ID HOST/SLAVE act_as_slave
15:08	Capabilities Pointer	8	0x60	R	Cap
7:0	Capability ID	8	0x08	R	HyperTransport capability ID

0x44

0x00112000

Link Config Link Control

14- 10 Link Config Link Control

30:28	Link Width Out	3	0x0	R/W	HT Disconnect 000 8 001 16
27	Reserved	1	0x0		
26:24	Link Width In	3	0x0	R/W	HT Disconnect

23	Dw Fc out	1	0x0	R	
22:20	Max Link Width out	3	0x1	R	HT 16bits
19	Dw Fc In	1	0x0	R	
18:16	Max Link Width In	3	0x1	R	HT 16bits
15:14	Reserved	2	0x0		
13	LDTSTOP# Tristate Enable	1	0x1	R/W	HT HT Disconnect HT PHY 1 0
12:10	Reserved	3	0x0		
9	CRC Error (hi)	1	0x0	R/W	8 CRC
8	CRC Error (lo)	1	0x0	R/W	8 CRC
7	Trans off	1	0x0	R/W	HT PHY 16 1 / 8 HT PHY 0 8 HT PHY 8 HT PHY bit 0
6	End of Chain	0	0x0	R	HT
5	Init Complete	1	0x0	R	HT
4	Link Fail	1	0x0	R	
3:2	Reserved	2	0x0		
1	CRC Flood Enable	1	0x0	R/W	CRC flood HT
0	Trans off (hi)	1	0x0	R/W	16 HT 8 8 PHY 1 8 HT PHY 0 8 HT PHY

0x4C

0x80250023

Revision ID Link Freq Link Error Link Freq Cap

14- 11 Revision ID Link Freq Link Error Link Freq Cap

31:16	Link Freq Cap	16	0x0000	R	HT PLL PLL 0x1F4 {3.2G,2.6G,2.4G,2.2G,2.0G,1.8G,1.6G, 1.4G,1.2G,1.0G,800M,600M,500M,400 M,300M,200M}

15:14	Reserved	2	0x0		
13	Over Flow Error	1	0x0	R	HT
12	Protocol Error	1	0x0	R/W	HT
11:8	Link Freq	4	0x0	R/W	HT HT Disconnect Link Freq Cap PLL 0x1F4
7:0	Revision ID	8	0x60	R/W	3.0

0x50
0x00000002
Feature Capability

14- 12 Feature Capability

31:9	Reserved	23	0x0		
8	Extended Register	1	0x0	R	
7:4	Reserved	3	0x0		
3	Extended CTL Time	1	0x0	R	
2	CRC Test Mode	1	0x0	R	
1	LDTSTOP#	1	0x1	R	LDTSTOP#
0	Isochronous Mode	1	0x0	R	

14.5.3 Error Retry

HyerTransport 3.0 Short Retry
Retry

0x64
0x00000000
Error Retry

14- 13 Error Retry

31:10	Reserved	22	0x0	R	

9	Retry Count Rollover	1	0x0	R	Retry
8	Reserved	1	0x0	R	
7:6	Short Retry Attempts	2	0x0	R/W	Short Retry
5:1	Reserved	5	0x0	R	
0	Link Retry Enable	1	0x0	R/W	

14.5.4 Retry Count

HyerTransport 3.0 m(شی

0x80000008

Interrupt Capability

14- 16 Interrupt Capability

31:24	Capabilities Pointer	8	0x80	R	Interrupt discovery and configuration block
23:16	Index	8	0x0	R/W	
15:8	Capabilities Pointer	8	0x0	R	Capabilities Pointer
7:0	Capability ID	8	0x08	R	Hypertransport Capablity ID

0x74

0x00000000

Dataport

14- 17 Dataport

31:0	Dataport	32	0x0	R/W	Index 0x10 0xa8 0xac

0x78

0xF8000000

IntrInfo[31:0]

14- 18 IntrInfo 1

31:24	IntrInfo[31:24]	8	0xF8	R	
23:2	IntrInfo[23:2]	22	0x0	R/W	IntrInfo[23:2] PIC IntrInfo
1:0	Reserved	2	0x0	R	

0x7c

0x00000000

IntrInfo[63:32]

14- 19 IntrInfo 2

31:0	IntrInfo[63:32]	32	0x0	R	

14.5.7

256 HT Fix Arbiter PIC

256 SMI NMI INIT INTA INTB INTC INTD

0x50 [28:24] 8 {INTD

INTC INTB INTA 1'b0 INIT NMI SMI} {Interrupt Index,

[2:0]}

256 4 8 HT

ht_int_8bit 256 8

256

	Strip	0	1	2	3	4	5	6	7
4	1	[X]	[X+64]	[X+128]	[X+192]	-	-	-	-
X = [63:0]	2	[2X]	[2X+1]	[2X+128]	[2X+129]	-	-	-	-
	4	[4X]	[4X+1]	[4X+2]	[4X+3]	-	-	-	-
8	1	[X]	[Y]	[X+64]	[Y+64]	[X+128]	[Y+128]	[X+192]	[Y+192]
X = [31:0]	2	[2X]	[2Y]	[2X+1]	[2Y+1]	[2X+128]	[2Y+128]	[2X+129]	[2Y+129]
Y = [63:32]	4	[4X]	[4X+32]	[4X+1]	[4X+33]	[4X+2]	[4X+34]	[4X+3]	[4X+35]

4

ht_int_stripe_1:

[0,1,2,3.....63] 0 /HT HI 4

[64,65,66,67.....127] 1 /HT HI 5

[128,129,130,131.....191] 2 /HT HI 6

[192,193,194,195.....255] 3 /HT HI 7

ht_int_stripe_2:

[0,2,4,6.....126] 0 /HT HI 4

[1,3,5,7……127] 1 /HT HI 5

[128,130,132,134……254] 2 /HT HI 6

[129,131,133,135……255] 3 /HT HI 7

ht_int_stripe_4:

[0,4,8,12……252] 0 /HT HI 4

[1,5,9,13……253] 1 /HT HI 5

[2,6,10,14……254] 2 /HT HI 6

[3,7,11,15……255] 3 /HT HI 7

ht_int_stripe_1

0x80

0x00000000

HT [31:0]

14- 20 HT 1

31:0	Interrupt_case [31:0]	32	0x0	R/W	HT [31:0] 0 /HT HI 4

0x84

0x00000000

HT [63:32]

14- 21 HT 2

31:0	Interrupt_case [63:32]	32	0x0	R/W	HT [63:32] 0 /HT HI 4

0x88

0x00000000

HT [95:64]

14- 22 HT 3

31:0	Interrupt_case [95:64]	32	0x0	R/W	HT [95:64] 1 /HT HI 5

0x8c
0x00000000
HT [127:96]

14- 23 HT 4

31:0	Interrupt_case [127:96]	32	0x0	R/W	HT [127:96] 1 /HT HI 5

0x90
0x00000000
HT [159:128]

14- 31 HT 5

31:0	Interrupt_case [159:128]	32	0x0	R/W	HT [159:128] 2 /HT HI 6

0x94
0x00000000
HT [191:160]

14- 24 HT 6

31:0	Interrupt_case [191:160]	32	0x0	R/W	HT [191:160] 2 /HT HI 6

0x98
0x00000000
HT [223:192]

14- 25 HT 7

31:0	Interrupt_case [223:192]	32	0x0	R/W	HT [223:192] 3 /HT HI 7

0x9c

0x00000000

HT [255:224]

14

0xa0
0x00000000
HT [31:0]

14- 27 HT 1

31:0	Interrupt_mask [31:0]	32	0x0	R/W	HT [31:0] 0 /HT HI 4

0xa4
0x00000000
HT [63:32]

14- 28 HT 2

31:0	Interrupt_mask [63:32]	32	0x0	R/W	HT [63:32] 0 /HT HI 4

0xa8
0x00000000
HT [95:64]

14- 29 HT 3

31:0	Interrupt_mask [95:64]	32	0x0	R/W	HT [95:64] 1 /HT HI 5

0xac
0x00000000
HT [127:96]

14- 30 HT 4

31:0	Interrupt_mask [127:96]	32	0x0	R/W	HT [127:96] 1 /HT HI 5

0xb0

0x00000000

HT [159:128]

14- 31 HT 5

31:0	Interrupt_mask [159:128]	32	0x0	R/W	HT [159:128] 2 /HT HI 6

0xb4

0x00000000

HT [191:160]

14- 32 HT 6

31:0	Interrupt_mask [191:160]	32	0x0	R/W	HT [191:160] 2 /HT HI 6

0xb8

0x00000000

HT [223:192]

14- 33 HT 7

31:0	Interrupt_mask [223:192]	32	0x0	R/W	HT [223:192] 3 /HT HI 7

0xbc

0x00000000

HT [255:224]

14- 34 HT 8

31:0	Interrupt_mask [255:224]	32	0x0	R/W	HT [255:224] 3 /HT HI 7

14.5.9 Link Train

HyperTransport 3.0

0xD0

0x00000070

Link Train

14- 35 Link Train

31:23	Reserved	9	0x0	R	
22 21	Transmitter LS select	2	0x0	R/W	Disconnected Inactive 2'b00 LS1 2'b01 LS0 2'b10 LS2 2'b11 LS3
14	Dsiable Cmd Throttling	1	0x0	R/W	HyperTransport 3.0 4 DWS Non-info CMD 1'b0 Cmd Throttling 1'b1 Cmd Ñr " kئ

HT P2P HT P2P

HT P2P HT CPU

P2P HT

0x140

0x00000000

HT 0

14- 36 HT 0

31	ht_rx_image0_en	1	0x0	R/W	HT 0
30	ht_rx_image0_trans_en	1	0x0	R/W	HT 0
29	ht_rx_image0_multi_node_en	1	0x0	R/W	HT 0 [39:37] [46:44]
28	ht_rx_image0_conf_hit_en	1	0x0	R/W	HT 0 0
25:0	ht_rx_image0_trans[49:24]	26	0x0	R/W	HT 0 [49:24]

0x144

0x00000000

HT 0

14- 37 HT 0

31:16	ht_rx_image0_base[39:24]	16	0x0	R/W	HT 0	[39:24]
15:0	ht_rx_image0_mask[39:24]	16	0x0	R/W	HT 0	[39:24]

0x148

0x00000000

HT 1

14- 38 HT 1

31	ht_rx_image1_en	1	0x0	R/W	HT 1
30	ht_rx_image1_trans_en	1	0x0	R/W	HT 1

29	ht_rx_image1_multi_node_en	1	0x0	R/W	HT 1 [39:37] [46:44]
28	ht_rx_image1_conf_hit_en	1	0x0	R/W	HT 1 0
25:0	ht_rx_image1_trans[49:24]	26	0x0	R/W	HT 1 [49:24]

0x14c
0x00000000
HT 1

14- 39 HT 1

31:16	ht_rx_image1_base[39:24]	16	0x0	R/W	HT 1 [39:24]
15:0	ht_rx_image1_mask[39:24]	16	0x0	R/W	HT 1 [39:24]

0x150
0x00000000
HT 2

14- 40 HT 2

31	ht_rx_image2_en	1	0x0	R/W	HT 2
30	ht_rx_image2_trans_en	1	0x0	R/W	HT 2
29	ht_rx_image2_multi_node_en	1	0x0	R/W	HT 2 [39:37] [46:44]
28	ht_rx_image2_conf_hit_en	1	0x0	R/W	HT 2 0
25:0	ht_rx_image2_trans[49:24]	26	0x0	R/W	HT 2 [49:24]

0x154
0x00000000
HT 2

14- 41 HT 2

31:16	ht_rx_image2_base[39:24]	16	0x0	R/W	HT	2	[39:24]
15:0	ht_rx_image2_mask[39:24]	16	0x0	R/W	HT	2	[39:24]

0x158
0x00000000
HT 3

14- 42 HT 3

31	ht_rx_image3_en	1	0x0	R/W	HT	3	
30	ht_rx_image3_trans_en	1	0x0	R/W	HT	3	
29	ht_rx_image3_multi_node_en	1	0x0	R/W	HT	3 [39:37] [46:44]	
28	ht_rx_image3_conf_hit_en	1	0x0	R/W	HT	3 0	
25:0	ht_rx_image3_trans[49:24]	26	0x0	R/W	HT	3	[49:24]

0x15C
0x00000000
HT 3

14- 43 HT 3

31:16	ht_rx_image3_base[39:24]	16	0x0	R/W	HT	3	[39:24]
15:0	ht_rx_image3_mask[39:24]	16	0x0	R/W	HT	3	[39:24]

0x160
0x00000000
HT 4

14- 44 HT 4

31	ht_rx_image4_en	1	0x0	R/W	HT	4	
30	ht_rx_image4_trans_en	1	0x0	R/W	HT	4	

29	ht_rx_image4_multi_node_en	1	0x0	R/W	HT 4 [39:37] [46:44]
28	ht_rx_image4_conf_hit_en	1	0x0	R/W	HT 4 0
25:0	ht_rx_image4_trans[49:24]	26	0x0	R/W	HT 4 [49:24]

0x164
0x00000000
HT 4

14- 45 HT 4

31:16	ht_rx_image4_base[39:24]	16	0x0	R/W	HT	4	[39:24]
15:0	ht_rx_image4_mask[39:24]	16	0x0	R/W	HT	4	[39:24]

14.5.11

HT

0x168
0x00000000

14- 46

31	ht_rx_header_trans_ext	1	0x1	R/W	0xFD_FE000000 type1 24 28 EXT HEADER
30	ht_rx_header_trans_en	1	0x1	R/W	0xFD_FE000000 [39:24]
29:0	ht_rx_header_trans[53:24]	30	0xFE00	R/W	[53:24] [53:25]

0x16C
0x00000000

14- 47

30	ht_rx_ext_header_trans_en	1	0x0	R/W	0xFE_00000000 [39:28]
29:0	ht_rx_ext_header_trans[53:24]	30	0x0	R/W	[53:24] [53:29]

14.5.12 POST

14.5.10

AXI AXI B

POST WRITE HT NONPOST

WRITE HT HT AXI

0x170

0x00000000

HT POST 0

14- 48 HT POST 0

31	ht_post0_en	1	0x0	R/W	HT POST 0
30	ht_split0_en	1	0x0	R/W	HT (CPU uncache ACC)
29:23	Reserved	14	0x0		
15:0	ht_post0_trans[39:24]	16	0x0	R/W	HT POST 0 [39:24]

0x174

0x00000000

HT POST 0

14- 49 HT POST 0

31:16	ht_post0_base[39:24]	16	0x0	R/W	HT POST 0 [39:24]

15:0	ht_post0_mask[39:24]	16	0x0	R/W	HT POST 0 [39:24]

0x178
0x00000000
HT POST 1

14- 50 HT POST 1

31	ht_post1_en	1	0x0	R/W	HT POST 1
30	ht_split1_en	1	0x0	R/W	HT (CPU uncache ACC)
29:16	Reserved	14	0x0		
15:0	ht_post1_trans[39:24]	16	0x0	R/W	HT POST 1 [39:24]

0x17c
0x00000000
HT POST 1

14- 51 HT POST 1

31:16	ht_post1_base[39:24]	16	0x0	R/W	HT POST 1 [39:24]
15:0	ht_post1_mask[39:24]	16	0x0	R/W	HT POST 1 [39:24]

14.5.13

14.5.10

AXI CACHE

HT CACHE HT

0x180
0x00000000
HT 0

14- 52 HT 0

31	ht_prefetch0_en	1	0x0	R/W	HT	0	
30:16	Reserved	15	0x0				
15:0	ht_prefetch0_trans[39:24]	16	0x0	R/W	HT	0	[39:24]

0x184
0x00000000
HT 0

14- 53 HT 0

31:16	ht_prefetch0_base[39:24]	16	0x0	R/W	HT	0	[39:24]
15:0	ht_prefetch0_mask[39:24]	16	0x0	R/W	HT	0	[39:24]

0x188
0x00000000
HT 1

14- 54 HT 1

31	ht_prefetch1_en	1	0x0	R/W	HT	1	
30:16	Reserved	15	0x0				
15:0	ht_prefetch1_trans[39:24]	16	0x0	R/W	HT	1	[39:24]

0x18c
0x00000000
HT 1

14- 55 HT 1

31:16	ht_prefetch1_base[39:24]	16	0x0	R/W	HT	1	[39:24]
15:0	ht_prefetch1_mask[39:24]	16	0x0	R/W	HT	1	[39:24]

14.5.14 UNCACHE

14.5.10

HT

SCACHE CACHE

IO CACHE

CACHE

30	ht_uncache1_trans_en	1	0x0	R/W	HT uncache 1
29	ht_uncache1_multi_node_en	1	0x0	R/W	HT uncache 1
28	ht_uncache1_conf_hit_en	1	0x0	R/W	HT uncache 1
25:0	ht_uncache1_trans[49:24]	26	0x0	R/W	HT uncache 1 [49:24]

0x19c
0x00000000
HT Uncache 1

14- 59 HT Uncache 1

31:16	ht_uncache1_base[39:24]	16	0x0	R/W	HT	uncache	1	[39:24]
15:0	ht_uncache1_mask[39:24]	16	0x0	R/W	HT	uncache	1	[39:24]

0x1A0
0x00000000
HT Uncache 2

14- 60 HT Uncache 2

31	ht_uncache2_en	1	0x0	R/W	HT	uncache	2
30	ht_uncache2_trans_en	1	0x0	R/W	HT	uncache	2
29	ht_uncache2_multi_node_en	1	0x0	R/W	HT	uncache	2
28	ht_uncache2_conf_hit						

14- 61 HT Uncache 2

31:16	ht_uncache2_base[39:24]	16	0x0	R/W	HT	uncache	2	[39:24]
15:0	ht_uncache2_mask[39:24]	16	0x0	R/W	HT	uncache	2	[39:24]

0x1B0
0x00000000
HT P2P 0

14- 64 HT P2P 0

31	ht_rx_p2p0_en	1	0x0	R/W	HT	P2P	0	
29:0	ht_rx_p2p0_trans[53:24]	30	0x0	R/W	HT	P2P	0	[53:24]

0x1B4
0x00000000
HT P2P 0

14- 65 HT P2P 0

31:16	ht_rx_p2p0_base[39:24]	16	0x0	R/W	HT	P2P	1	[39:24]
15:0	ht_rx_p2p0_mask[39:24]	16	0x0	R/W	HT	P2P	1	[39:24]

0x1B8
0x00000000
HT P2P 1

14- 66 HT P2P 1

31	ht_rx_p2p1_en	1	0x0	R/W	HT	P2P	1	
29:0	ht_rx_p2p1_trans[53:24]	30	0x0	R/W	HT	P2P	1	[53:24]

0x1BC
0x00000000
HT P2P 1

14- 67 HT P2P 1

31:16	ht_rx_p2p1_base[39:24]	16	0x0	R/W	HT	P2P	1	[39:24]
15:0	ht_rx_p2p1_mask[39:24]	16	0x0	R/W	HT	P2P	1	[39:24]

14.5.16

0x1C0
0x00904321
APP CONFIG 0

14- 68 0

31:30	Reserved	1	0x0		
29	Ldt Stop Gen	1			

					0xF

0x1C4
0x00904321
APP CONFIG1

14- 69 1

31	tx post split en	1	0x0	R/W	tx post ID 32 byte write
30	tx wr passPW pc	1	0x0	R/W	Post passPW 1
29	tx wr passPW npc	1	0x0	R/W	Nonpost passPW 1
28	tx rd passPW	1	0x0	R/W	passPW 1
27	stop same id wr	1	0x0	R/W	AXI ID ID
26	stop same id rd	1	0x0	R/W	AXI ID ID
25	Not axi2seqid wr	1	0x0	R/W	AXI ID seqid fixed seqid
24	Not axi2seqid rd	1	0x0	R/W	AXI ID seqid fixed seqid
23:22	Reserved	2	0x0	R/W	
21	act as slave	1	0x1	R/W	SLAVE
20	Host hide	1	0x0	R/W	
19:16	Rrequest delay	4	0x3	R/W	Rrequest 000 0 001 0-8 010 8-15 011 16-31 100 32-63 101 64-127 110 128-255 111 0

15	Crc Int en	1	0x0	R/W	CRC
14:12	Crc Int route	3	0x0	R/W	CRC
11	Reserved				
10	ht int 8 bit	1	0x0	R/W	8
9:8	ht_int_stripe	2	0x0	R/W	3 0x0 ht_int_stripe_1 0x1 ht_int_stripe_2 0x2 ht_int_stripe_4
4:0	Interrupt Index	5	0x0	R/W	SMI NMI INIT INTA INTB INTC INTD 256 5 000 SMI 001 NMI 010 INIT 011 Reserved 100 INTA 101 INTB 110 INTC 111 INTD

14.5.17

0x1C8

0x00000000

14- 70

31:16	rx_cad_phase_0	16	0x0	R/W	CAD[15:0]
15:8	rx_ctl_catch	8	0x0	R/W	ctl 0 2 4 6 CTL0 1 3 5 7 CTL1
7:0					

14.5.18 PHY

PHY

0x1CC

0x83308000

PHY

14- 71 PHY

31:29	Reserved	3	0x0	R	
28	dll locked hi	1	0x0	R	8 DLL
27	dll locked lo	1	0x0	R	8 DLL
26	cdr locked hi	1	0x0	R	8 CDR
25	cdr locked lo	1	0x0	R	8 CDR
24	phase locked	1	0x0	R	
23:20	phy state	4	0x0	R	PHY
19:17	tx training status	3	0x0	R	TX
16:14	rx training status	3	0x0	R	RX
13:8	Init done	6	0x0	R	
7:0	Reserved	8		R	

14.5.19

0x1D0

0x00000000

14- 72

31:24	B_CMD_txbuffer	8	0x0	R	B
23:16	R_CMD_txbuffer	8	0x0	R	R
15:8	NPC_CMD_txbuffer	8	0x0	R	NPC
7:0	PC_CMD_txbuffer	8	0x0	R	PC

14.5.20

0x1D4
0x00000000

14- 73

31	Reserved	1	0x0	R	
30	rx_buffer_r_data[4]	1	0x0	R/W	buffer bit[4]
29	rx_buffer_npc_data[4]	1	0x0	R/W	npc buffer bit[4]
28	rx_buffer_pc_data[4]	1	0x0	R/W	pc buffer bit[4]
27	rx_buffer_b_cmd[4]	1	0x0	R/W	bresponse buffer bit[4]
26	rx_buffer_r_cmd[4]	1	0x0	R/W	buffer bit[4]
25	rx_buffer_npc_cmd[4]	1	0x0	R/W	npc buffer bit[4]
24	rx_buffer_pc_cmd[4]	1	0x0	R/W	pc buffer bit[4]
23:16	R_DATA_txbuffer	8	0x0	R	R
15:8	NPC_DATA_txbuffer	8	0x0	R	NPC
7:0	PC_DATA_txbuffer	8	0x0	R	PC

14.5.21

HT

0x1D8
0x00000000

14- 74

31	b_interleave	1	0x0	R/W	B
30	nop_interleave	1	0x0	R/W	
29	Tx_neg	1	0x0	R/W	0 1 +1
28	Tx_buff_adj_en	1	0x0	R/W	0->1
27:24	R_DATA_txadj	4	0x0	R/W	R tx_neg 0 R_DATA_txadj tx_neg 1 R_DATA_txadj+1
23:20	NPC_DATA_txadj	4	0x0	R/W	NPC tx_neg 0 NPC_DATA_txadj tx_neg 1 NPC_DATA_txadj+1
19:16	PC_DATA_txadj	4	0x0	R/W	PC tx_neg 0 PC_DATA_txadj tx_neg 1 PC_DATA_txadj+1
15:12	B_CMD_txadj	4	0x0	R/W	B tx_neg 0 B_CMD_txadj tx_neg 1 B_CMD_txadj+1
11:8	R_CMD_txadj	4	0x0	R/W	R tx_neg 0 R_CMD_txadj tx_neg 1 R_CMD_txadj+1
7:4	NPC_CMD_txadj	4	0x0	R/W	NPC / tx_neg 0 NPC_CMD_txadj tx_neg 1 NPC_CMD_txadj+1
3:0	PC_CMD_txadj	4	0x0	R/W	PC tx_neg 0 PC_CMD_txadj tx_neg 1 PC_CMD_txadj+1

14.5.22

0x1DC

0x07778888

14- 75

27:24	rx_buffer_r_data	4	0x0	R/W	buffer
23:20	rx_buffer_npc_data	4	0x0	R/W	npc buffer
19:16	rx_buffer_pc_data	4	0x0	R/W	pc buffer
15:12	rx_buffer_b_cmd	4	0x0	R/W	bresponse buffer
11:8	rx_buffer_r_cmd	4	0x0	R/W	buffer
7:4	rx_buffer_npc_cmd	4	0x0	R/W	npc buffer
3:0	rx_buffer_pc_cmd	4	0x0	R/W	pc buffer

14.5.23 Training 0

HyerTransport 3.0 Training 0

HyperTransport3.0 1/4

0x1E0

0x00000080

Training 0

14- 76 Training 0

31	Gen3_timing_soft	1	0x0	R/W	
30:23	Retry_nop_num	8	0x0	R/W	
22:0	T0 time	23	0x80	R/W	Training 0

14.5.24 Training 0

HyerTransport 3.0 Training 0

HyperTransport3.0 1/4

0x1E4

0x000fffff

Training 0

14- 77 Training 0

31:0	T0 time	32	0xfffff	R/W	Training 0

14.5.25 Training 1

HyerTransport 3.0 Training 1

HyperTransport3.0 1/4

0x1E8

0x0004fffff

Training 1

14- 78 Training 1

31:0	T1 time	32	0x4fffff	R/W	Training 1 ¢

31:0	T3 time	32	0x7fffff	R/W	Training 3

14.5.28

PLL

1

PLL div_refc div_loop ,

phy_hi_div phy_lo_div core_div warm

reset LDT disconnect PLL

PHY_LINK_CLK HT

SYS_CLOCK

0x00000000

14- 81

31 27	PLL relock counter	5	0x0	R/W	counter select {PLL_relock_counter ,5 ' h1f} 10 ' 3ff
26	Counter select	1	0x0	R/W	1 ' b0 1 ' b1 PLL_relock_counter
25	Reserved	1	0x0	R	
24 16	Soft_div_loop	7	0x0	R/W	PLL
15 12	Soft_div_refc	4	0x0	R/W	PLL
11 8	Soft_phy_hi_div	4	0x0	R/W	PHY
7 4	Soft_phy_lo_div	4	0x0	R/W	PHY
3	Locked	1	0x0	R	
2	Reserved	1	0x0	R	
1	Soft cofig enable	1	0x0	R/W	1 ' b0 1 ' b1
0	Reserved	1	0x0	R	

14.5.29 PHY

PHY

0x1F8

0x00000000

PHY

14- 82

31	Tx_scanin_en	1	0x0	R/W	TX
30	Rx_scanin_en	1	0x0	R/W	RX
27:24	Tx_scanin_ncode	4	0x0	R/W	TX ncode

23:20	Tx_scanin_pcode	4	0x0	R/W	TX pcode
19:12	Rx_scanin_code	8	0x0	R/W	RX

14.5.30 PHY

PHY 8bit

PHY PHY 1 16bit

PHY

0x1FC

0x83308000

PHY

14- 83 PHY

31	Rx_ckpll_term	1	0x1	R/W	PLL RX
30	Tx_ckpll_term	1	0x0	R/W	PLL TX
29	Rx_clk_in_sel_	1	0x0	R/W	PAD PAD HT1 CLKPAD: 1'b0 1'b1 PLL
28	Rx_ckdll_sell	1	0x0	R/W	DLL 1'b0 PLL 1'b1
27:26	Rx_ctle_bitc	2	0x0	R/W	PAD EQD
25:24	Rx_ctle_bitr	2	0x3	R/W	PAD EQD
23:22	Rx_ctle_bitlim	2	0x0	R/W	PAD EQD
21	Rx_etN				

16:12	Tx_preenmp	5	0x08	R/W	PAD
11 0	Reserved	12	0x0	R	

14.5.31

HyperTransport 3.0 PHY CDR lock CDR

CDR

0x240
0x00000000

14- 84

15	Cdr_ignore_enable	1	0x0	R/W	CRC lock 1 ' b0 CDR lock 1 ' b1 CDR lock
14 0	Cdr_wait_counter	15	0x0	R/W	

14.5.32 LDT

LDT reconnect

LDT ,

0x244
0x00000000
LDT 1

14- 85 LDT 1

31:16	Rx_wait_time	16	0x0	R/W	RX
15:0	Tx_wait_time	16	0x0	R/W	TX

14- 90 LDT 5

31:0	wait cad	32	0x0	R/W	

14.5.33 HT TX POST ID

ID HT POST

0x260
0x00000000
HT TX POST ID WIN0

14- 91 HT TX POST ID WIN0

31:16	HT TX POST ID0 MASK	16	0x0	R/W	AXI ID POST ID MASK
15:0	HT TX POST ID0 BASE	16	0x0	R/W	AXI ID POST ID BASE

0x264
0x00000000
HT TX POST ID WIN1

14- 92 HT TX POST ID WIN1

31:16	HT TX POST ID1 MASK	16	0x0	R/W	AXI ID POST ID MASK
15:0	HT TX POST ID1 BASE	16	0x0	R/W	AXI ID POST ID BASE

0x268
0x00000000
HT TX POST ID WIN2

14- 93 HT TX POST ID WIN2

31:16	HT TX POST ID2 MASK	16	0x0	R/W	AXI ID POST ID MASK

15:0	HT TX POST ID2 BASE	16	0x0	R/W	AXI ID POST ID BASE

0x26C
0x00000000
HT TX POST ID WIN3

14- 94 HT TX POST ID WIN3

31:16	HT TX POST ID3 MASK	16	0x0	R/W	AXI ID POST ID MASK
15:0	HT TX POST ID3 BASE	16	0x0	R/W	AXI ID POST ID BASE

14.5.34

HT IO

HT IO

0x270
0x00000000
HT RX INT TRANS Lo

14- 95 HT RX INT TRANS LO

31:4	INT_trans_addr[31:4]	28	0x0	R/W	
3:0	Reserved	4	0x0	R	

0x274
0x00000000
HT RX INT TRANS Hi

14- 96 HT RX INT TRANS Hi

31	INT_trans_en	1	0x0	R/W	
30	INT_trans_allow	1	0x0	R/W	INT_trans_en EXT_INT_en

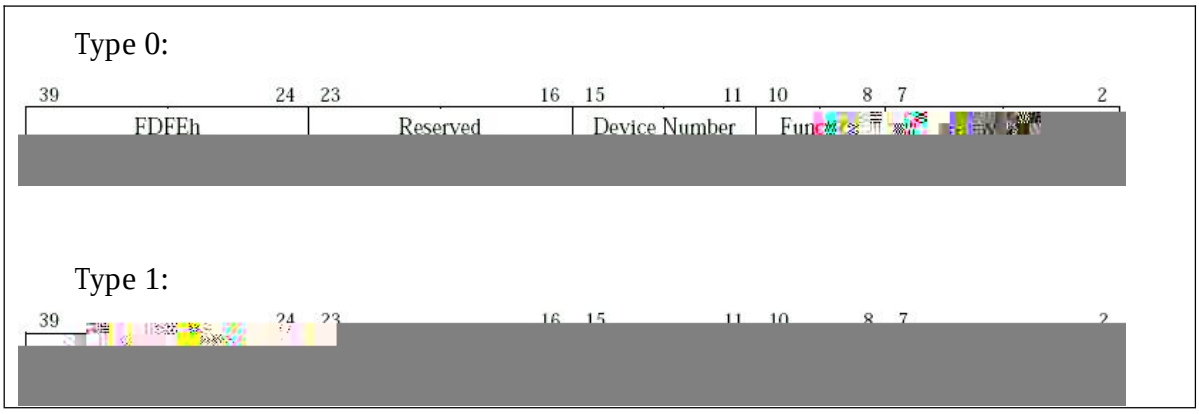
29:26	INT_trans_cache	4	0x0	R/W	Cache
25:0	INT_trans_addr[57:32]	26	0x0	R/W	

14.6 HyperTransport

HyperTransport PCI

14- 6 HT

0xFD_FE00_0000 0xFD_FFFF_FFFF HT 3C5000L



14- 1 3C5000L HT

15 IO

3 I/O UART SPI I2C GPIO I/O

AXI CPU

15.1 UART

UART

- /
-
- 16
-
-
- FIFO
- NS16550A

UART

UART0 0x1FE001E0

UART1 0x1FE001E8

UART 0x1FE00100(UART0)

0x1FE00110(UART1) RFC TFC

15.1.1 DAT

[7 0]

0x00

0x00

7:0	Tx FIFO	8	W	

15.1.2 IER

[7 0]

0x01

0x00

7:4	Reserved	4	RW	
3	IME	1	RW	Modem ‘0’ – ‘1’ –
2	ILE	1	RW	‘0’ – ‘1’ –
1	ITxE	1	RW	‘0’ – ‘1’ –
0	IRxE	1	RW	‘0’ – ‘1’ –

15.1.3 IIR

[7 0]

0x02

0xc1

7:4	Reserved	4	R	
3:1	II	3	R	
0	INTp	1	R	

Bit 3	Bit 2	Bit 1				

0	1	1	1st			LSR
0	1	0	2nd		FIFO trigger	FIFO trigger
1	1	0	2nd		FIFO 4	FIFO
0	0	1	3rd			THR IIR
0	0	0	4th	Modem	CTS, DSR, RI or DCD.	MSR

15.1.4 FIFO FCR

FIFO

[7 0]

0x02

0xc0

7:6	TL	2	W	FIFO trigger ‘00’ – 1 ‘01’ – 4 ‘10’ – 8 ‘11’ – 14
5:3	Reserved	3	W	
2	Txset	1	W	‘1’ FIFO
1	Rxset	1	W	‘1’ FIFO

0	Reserved	1	W	

15.1.5 LCR

[7 0]

0x03

0x03

7	dlab	1	RW	‘1’ – ‘0’ –
6	bcb	1	RW	‘1’ – 0( ). ‘0’ –
5	spb	1	RW	‘0’ – ‘1’ – LCR[4] 1 0 LCR[4] 0 1
4	eps	1	RW	‘0’ – 1 ‘1’ – 1

3	pe	1	RW	‘0’ – ‘1’ –
2	sb	1	RW	‘0’ – 1 ‘1’ – 5 1.5 2
1:0	bec	2	RW	‘00’ – 5 ‘01’ – 6 ‘10’ – 7 ‘11’ – 8

15.1.6 MODEM MCR

Modem

[7 0]

0x04

0x00

7:5	Reserved	3	W	
4	Loop	1	W	‘0’ – ‘1’ – TXD 1

				DTR Č DSR RTS Č CTS Out1 Č RI Out2 Č DCD
3	OUT2	1	W	DCD
2	OUT1	1	W	RI
1	RTSC	1	W	RTS
0	DTRC	1	W	DTR

15.1.7 LSR

[7 0]

0x05

0x00

7	ERROR	1	R	‘1’ – ‘0’ –
6	TE	1	R	‘1’ – FIFO

				FIFO ‘0’ –
5	TFE	1	R	FIFO ‘1’ – FIFO FIFO ‘0’ –
4	BI	1	R	‘1’ – 0 ‘0’ –
3	FE	1	R	‘1’ – ‘0’ –
2	PE	1	R	‘1’ – ‘0’ –
1	OE	1	R	‘1’ – ‘0’ –
0	DR	1	R	‘0’ – FIFO ‘1’ – FIFO

LSR[0] FIFO

15.1.8 MODEM MSR

Modem

[7 0]

0x06

0x00

7	CDCD	1	R	DCD Out2
6	CRI	1	R	RI OUT1
5	CDSR	1	R	DSR DTR
4	CCTS	1	R	CTS RTS
3	DDCD	1	R	DDCD
2	TERI	1	R	RI RI
1	DDSR	1	R	DDSR
0	DCTS	1	R	DCTS

15.1.9 FIFO RFC

FIFO

[7 0]

0x08

0x00

3C5000L

0x00

7:0	D_DIV	8	RW	

15.1.12

FIFO RFC CPU FIFO CPU

CPU UART

FIFO TFC CPU FIFO CPU

FIFO CPU UART

3

100MHz 16

MSB LSB 256 D_DIV

15.2 SPI

SPI

，

，4

，

，

，

，

，SPI

，SPI

，Dual/Quad mode SPI flash

SPI 0x1FE001F0

15- 1 SPI

SPI Boot	0X1FC0_0000-0X1FD0_0000	1MByte
SPI Memory	0X1D00_0000-0X1E00_0000	16MByte
SPI Register	0X1FE0_01F0-0X1FE0_01FF	16Byte

SPI Boot 0xBFC00000

SPI

SPI Memory CPU 1M SPI BOOT

15.2.1 SPCR

[7 0]

0x00

0x10

7	Spie	1	RW	
6	spe	1	RW	
5	Reserved	1	RW	
4	mstr	1	RW	master 1
3	cpol	1	RW	
2	cpha	1	RW	1 0
1:0	spr	2	RW	sclk_o sper spre

15.2.2 SPSR

[7 0]

0x01

0x05

7	spif	1	RW	1 1
6	wcol	1	RW	1 , 1
5:4	Reserved	2	RW	
3	wffull	1	RW	1
2	wfempty	1	RW	1
1	rffull	1	RW	1
0	rfempty	1	RW	1

15.2.3 TxFIFO

[7 0]

0x02

0x00

7:0	Tx FIFO	8	W	

15.2.4 SPER

[7 0]

0x03

0x00

7:6	icnt	2	RW	00 – 1 01 - 2 10 - 3 11 - 3
5:2	Reserved	4	RW	
1:0	spre	2	RW	Spr

spre	00	00	00	00	01	01	01	01	10	10	10	10
spr	00	01	10	11	00	01	10	11	00	01	10	11
	2	4	16	32	8	64	128	256	512	1024	2048	4096

15.2.5 SFC_PARAM

SPI Flash

[7 0]

0x04

0x21

7:4	clk_div	4	RW	{spre,spr}
3	dual_io	1	RW	I/O
2	fast_read	1	RW	
1	burst_en	1	RW	spi flash

0	memory_en	1	RW	spi flash csn[0]

15.2.6 SFC_SOFTCS

SPI Flash

[7 0]

0x05

0x00

7:4	csn	4	RW	csn
3:0	csen	4	RW	1 cs 7:4

15.2.7 SFC_TIMING

SPI Flash

[7 0]

0x06

0x03

7:4	Reserved	4	RW	
3	quad_io	1	RW	4 1
2	tFast	1	RW	
1:0	tCSH	2	RW	SPI Flash T 00: 1T 01: 2T 10: 4T 11: 8T

15.2.8 CTRL

SPI Flash

[7 0]

0x08

0x00

7:4	nbyte	4	RW	
3:2	reserve	2	RW	
1	nbmode	1	RW	
0	start	1	RW	

15.2.9 CMD

SPI Flash

[7 0]

0x09

0x00

7:0	cmd	8	RW	spi flash

15.2.10 0 BUF0

SPI Flash 0

[7 0]

0x0a

0x00

7:0	buf0	8	RW	SPI SPI

15.2.11 1 BUF1

SPI Flash 1

[7 0]

0x0b

0x00

7:0	buf1	8	RW	SPI SPI

15.2.12 0 TIMER0

SPI Flash 0

[7 0]

0x0c

0x00

7:0	time0	8	RW	8

15.2.13 1 TIMER1

SPI Flash 1

[7 0]

0x0d

0x00

7:0	time1	8	RW	8

15.2.14 2 TIMER2

SPI Flash 2

FLASH

15.3 I2C

I2C I2C

I2C SDA SCL

400kbps

3C5000L I2C

SLV_CTRL[6:0]

I2C0 0x1FE00120

I2C1 0x1FE00130

15.3.1 PRERlo

[7 0]

0x00

0xff

7:0	PRERlo	8	RW	8

15.3.2 PRERhi

[7 0]

0x01

0xff

7:0	PRERhi	8	RW	8

prescale LPB PCLK clock_aSCL

clock_s

Prcescale = clock_a/(4*clock_s)-1

15.3.3 CTR

[7 0]

0x02

0x20

7	EN	1	RW	1 , 0
6	IEN	1	RW	1
5	MST_EN	1	RW	0 slave 1 master
4:0	Reserved	5	RW	

15.3.4 TXR

[7 0]

0x03

0x00

7:1	DATA	7	W	
0	DRW	1	W	

15.3.5 RXR

[7 0]

0x03

0x00

7:0	RXR	8	R	

15.3.6 CR

[7 0]

0x04

0x00

7	STA	1	W	START
6	STO	1	W	STOP
5	RD	1	W	
4	WR	1	W	
3	ACK	1	W	
2:1	Reserved	2	W	
0	IACK	1	W	

I2C ‘0’ bit3 1

ack ack

15.3.7 SR

[7 0]

0x04

0x00

7	RxACK	1	R	1

				0
6	Busy	1	R	I2c 1 0
5	AL	1	R	I2C I2C 1
4:2	Reserved	3	R	
1	TIP	1	R	 1 0
0	IF	1	R	 1

15.3.8 SLV_CTRL

[7 0]

0x07

0x00

7	SLV_EN	1	WR	MST_EN 0
6 0	SLV_ADDR	7	WR	I2C